

APPLICATION OF THE μ A722 10-BIT CURRENT SOURCE

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INTRODUCTION

The purpose of this application note is threefold:

- (1) to describe the characteristics of the μ A722 in sufficient detail to enable advance designers to plan new subsystems around it;
- (2) to present standard trouble-free designs for D/A and A/D converters using the μ A722;
- (3) to suggest system applications of D/A and A/D converters, especially those made feasible for the first time by the combination of performance, economy, and miniaturization which the μ A722 and compatible IC's will offer.

Therefore, it is organized in three major sections, as follows:

- I. Operating Principles, Performance, and Interface Requirements of the μ A722.
- II. D/A-A/D Conversion and Other Subsystem Applications of the μ A722.
- III. System Applications of μ A722 Subsystems.

The treatment and style are intended to be comprehensive yet not exhaustive. Therefore, lengthy analyses and derivations have been omitted or relegated to the Appendix, in favor of directly useful information in the form of figures, tables, curves, and brief paragraphs outlining application principles and procedures.

I. OPERATING PRINCIPLES, PERFORMANCE AND INTERFACE REQUIREMENTS

General Description

The μ A722 is a high-speed, 10-bit precision current source intended for use in current-summing digital-to-analog converters or as the feedback element in successive approximation analog-to-digital converters. It is constructed on a single silicon chip, using the Fairchild Planar* epitaxial process, and consists of a

* Planar is a patented Fairchild process.

reference supply, 10 current sources connected to a single output summing line, and associated logic switches. The full-scale current and coding format are set by an external resistor array, which may be preselected and fixed for general usage or trimmed for greater accuracy. The μ A722 is compatible with all Fairchild digital circuits, and with most linear circuits such as the μ A702, μ A709, μ A710, μ A741, and μ A727.

SUMMARY OF TYPICAL OPERATING SPECIFICATIONS

Supply Voltages: V^+	+6 Volts to +12 Volts
V^-	-6 Volts to -12 Volts
Logic Levels: Source "ON"	$\leq +0.5$ Volts
Source "OFF"	$\geq +2$ Volts
Summing Line (Output) Potential	Virtual Ground ± 5 Volts
Emitter Resistors	See Table I
Resolution	1024 Parts
Range (Full-Scale)	0 to 2560 μ A
Speed	0.6 μ sec/bit
Accuracy: Full-Scale (-20°C to +85°C)	$\pm 0.2\%$ (including resistor tolerances)
Nonlinearity (+25°C)	$\pm 0.07\%$ (fixed resistors); zero (trimmed resistors)
Total Error (-20°C to +85°C)	$\pm 0.2\%$ (including resistor tolerances)
Package	24-Lead Flatpack (1/4" x 3/8")

Circuit Description

A converter requires either accurate voltage or current switching. Current switching was chosen because it is generally more compatible with both the advantages and limitations of integrated circuits. Major advantages are:

- (1) The excellent matching of collector current and base-emitter voltage permits accurately weighted currents to be generated that are stable over a wide range of temperatures.

* Full scale and nonlinearity errors are not additive (see Fig. 6).

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- (2) The current switching may be easily accomplished with excellent isolation between control and signal circuits without the use of capacitors or transformers.
- (3) The accuracy of current switching is relatively independent of the device characteristics.
- (4) The switching may be accomplished with acceptable speed using device structures compatible with linear integrated circuit requirements.

A simplified equivalent circuit for the $\mu A722$ is shown in Figure 1. The external resistor array sets the individual current source values. The bit control gates are controlled from the logic inputs with levels that are compatible with the various Fairchild Micrologic[®] integrated circuit families. The internal voltage reference establishes the proper bias for the current sources.

The basic circuit for each current source (Figure 2) consists of a level shifter (Q_{11} , D_{11} , and Q_{31}), a current steering network (Q_{21} , D_1), the current source transistor (Q_1), and an h_{FE} compensating circuit (Q_{41} , R_1). For maximum output impedance, the current source transistor is operated in a common base configuration. The value of the internal diffused emitter resistor (R_1) of Q_{41} was chosen to make the collector currents of Q_1 and Q_{41} approximately equal. If the two transistors are well-matched, their base currents will be equal and the collector current of Q_1 will be given by:

$$I_{C1} = \frac{V_B - V_{BE1}}{R_{E1}} \quad (1)$$

The bias voltage, V_B , is designed to have a temperature coefficient equal and opposite to that of V_{BE1} , so that the voltage across R_{E1} is held constant with temperature. Thus, I_{C1} may be accurately controlled by the external precision resistor independent of transistor h_{FE} and V_{BE} , provided Q_1 and Q_{41} are well-matched.

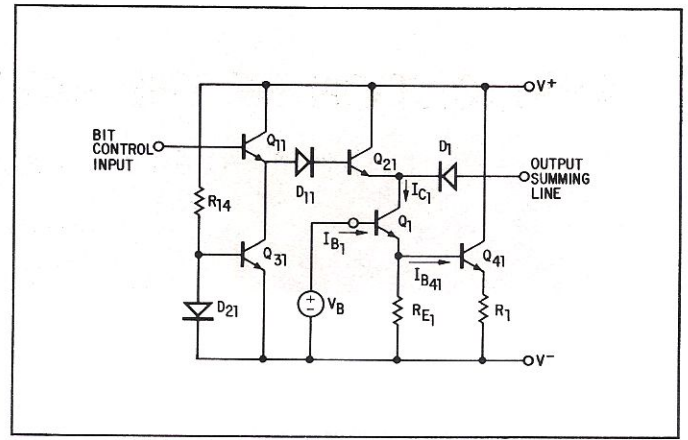


Fig. 2. Basic current source with switching network.

Switching is obtained by current steering. In order to be compatible with DTL, RTL, and CTL logic levels, a buffered level shifter is employed with the steering circuitry. When the logic level is high, the source current is provided from the logic side through Q_{21} , raising the collector voltage of Q_1 sufficiently to back-bias diode D_1 and thus keep the current out of the summing line. When the logic is low, the base of transistor Q_{21} is sufficiently negative with respect to the collector of Q_1 to turn off Q_{21} , allowing D_1 to be forward-biased, and drawing the current through the summing line. The converter consists of ten such current sources and switch networks, operating in parallel from a common reference supply. The complete circuit is shown in Figure 3.

The reference supply includes a stable voltage source and a voltage regulator. The regulator output provides the proper temperature compensating voltage reference level with a low source impedance. An external 200pF* capacitor is required at the frequency compensation terminal to protect against oscillation in the regulator.

* 200 pF is adequate; 1000 pF is best. See Fig. 13.

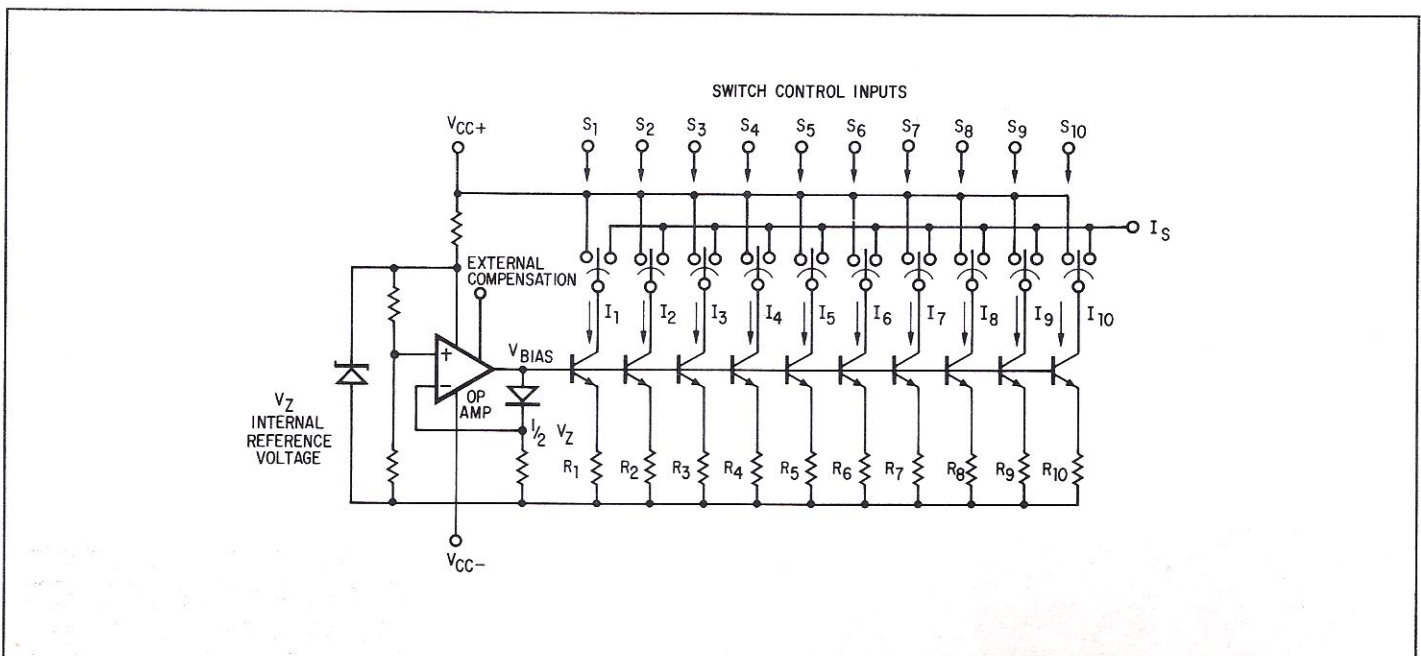


Fig. 1. Functional schematic: $\mu A722$ digital-to-analog converter current source.

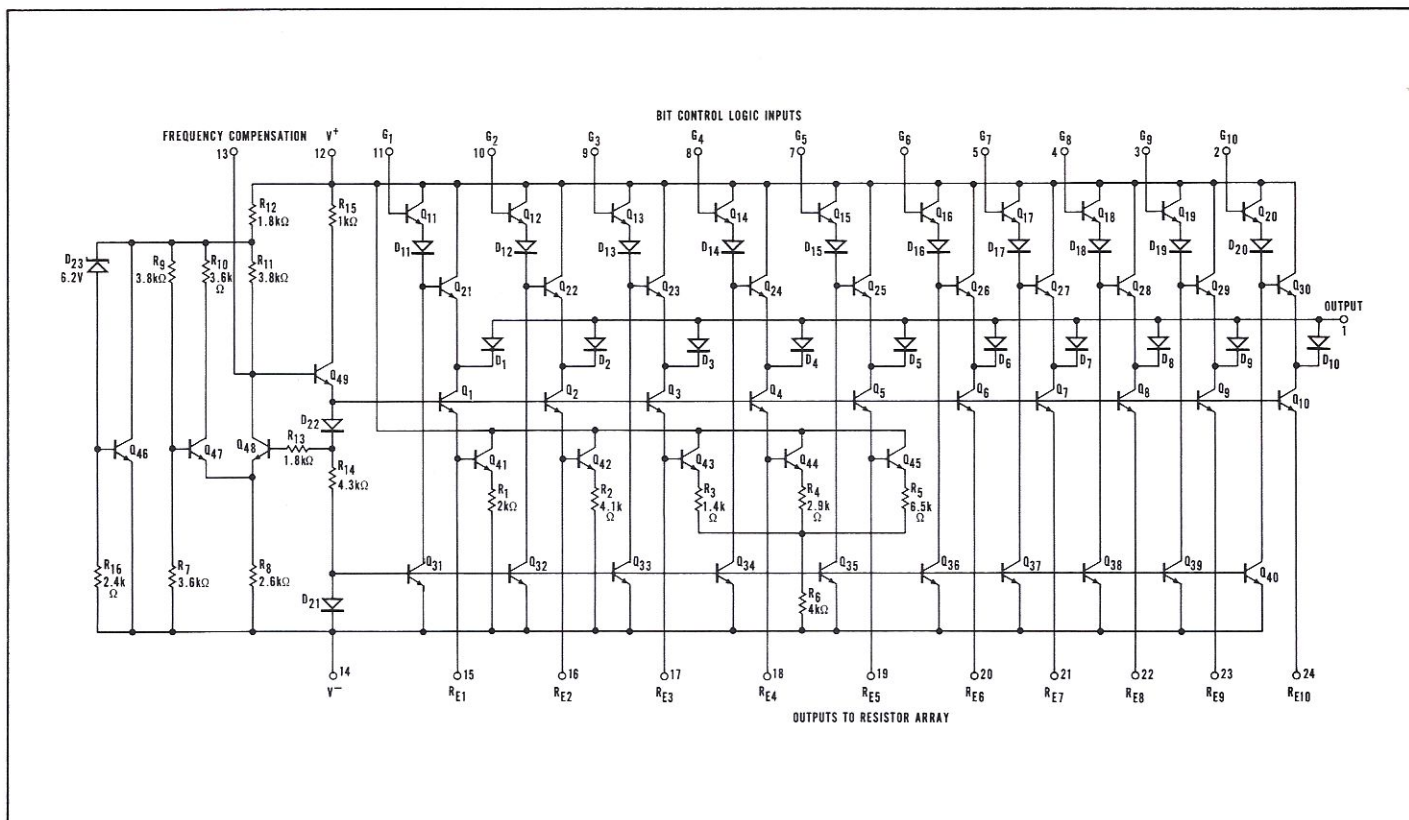


Fig. 3. Schematic diagram.

The converter maintains accuracy with ambient temperature variations as follows:

The regulator output versus temperature is tailored to maintain $V_B - V_{BE}$ constant. Diode D_{22} in the regulator feedback loop carries the same current density as the first two current source transistors, Q_1 and Q_2 . Diode D_{22} and transistor Q_2 have identical geometries and carry a nominal $640\mu A$. Transistor Q_1 has twice the emitter area of D_{22} and Q_2 , and hence carries $1280\mu A$. Therefore, D_{22} , Q_1 , and Q_2 have the same V_{BE} and the same V_{BE} temperature coefficient, thus maintaining the emitter voltages of Q_1 and Q_2 constant over temperature. Other subsequent current sources have geometries identical to Q_2 but carry binarily decreasing currents and therefore have slightly differing temperature coefficients. However, the error resulting from this mismatch is small.

The emitter-follower circuits, Q_{41} through Q_{45} , compensate for temperature-dependent changes in the base currents of the current source transistors by removing a similar current prior to the external emitter resistor. If the external emitter resistors are near their nominal value ($\pm 10\%$), errors due to beta mismatch between the source transistor and the compensating transistor are small, as are errors due to the tolerance on the diffused emitter resistors for Q_{41} through Q_{45} . Since the ratio of bit current to full-scale current decreases towards the least significant bit, this compensation is required only on the first 5 current sources.

The current source transistors have high betas at the current levels of the most significant bits. This results in a bias current drawn by the 10 sources that is small compared to the $640\mu A$ flowing in the regulator diode. This, coupled with a low

output impedance for the regulator, results in negligible reference voltage variations due to the temperature-dependent base currents of the current sources.

Diode D_{21} compensates temperature-dependent variations in R_{14} sufficiently to limit the current variations in diode D_{22} to less than $\pm 5\%$. The resulting variations in the reference voltage are small enough to permit operation over a wide temperature range.

Selection of Emitter Resistors

An examination of the binary code resistor array values (Table I) indicates that resistors R_{E3} to R_{E10} do not increase in an exact binary fashion. There are two reasons for this: first, the V_{BE} 's of current sources 3 to 10 do not match exactly the biasing diode voltage V_{D22} ; and second, the base currents of sources 6 to 10 are not compensated. The resistor array values given in Table I account for these factors and, if kept within the indicated tolerances, will give the overall accuracy specified for the converter. Recommended TCR values are given for accuracies ranging from 6 bits $\pm 1/2$ LSB to 9 bits $\pm 1/2$ LSB over the restricted military temperature range, $-20^\circ C$ to $+85^\circ C$. Obviously, they are conservative for reduced temperature ranges commonly specified for industrial and commercial equipment. The resistors R_{S1} , R_{S2} , and R_S' in Table I are discussed in the following subsections (see Eq. 1).

* Table I anticipates more accurate versions of the $\mu A722$ in the future.

TABLE IA.
BINARY CODE RESISTOR ARRAY

Resistor No.	Nominal Resistance Value k Ω	Nominal R/R _{E1} Ratio	6 Bit $\pm 1/2$ Bit Array Error = $\pm .8\%$ Error Allocated to Resistors = $\pm .16\%$		7 Bit $\pm 1/2$ Bit Array Error = $\pm .4\%$ Error Allocated to Resistors = $\pm .08\%$		8 Bit $\pm 1/2$ Bit Array Error = $\pm .2\%$ Error Allocated to Resistors = 400 ppm		9 Bit $\pm 1/2$ Bit Array Error = $\pm .1\%$ Error Allocated to Resistors = 200 ppm	
			Ratio Tolerance at 25°C %	T.C. max (-20°C -85°C) of Resistor Ratios ppm/°C	Ratio Tolerance at 25°C %	T.C. max (-20°C -85°C) of Resistor Ratios ppm/°C	Ratio Tolerance at 25°C %	T.C. max (-20°C -85°C) of Resistor Ratios ppm/°C	Ratio Tolerance at 25°C %	T.C. max (-20°C -85°C) of Resistor Ratios ppm/°C
RE1	2.547	1.000	$\pm 10.0^*$	± 50	$\pm 10.0^*$	± 50	$\pm 10.0^*$	± 20	$\pm 10.0^*$	± 20
RE2	5.094	2.000	± 10	± 20	± 10	± 20	± 10	± 5	± 10	± 5
RE3	10.24	4.022	± 20	± 50	± 05	± 20	± 05	± 10	± 02	± 5
RE4	20.60	8.088	± 20	± 50	± 10	± 20	± 10	± 20	± 05	± 10
RE5	41.43	16.26	± 50	± 100	± 20	± 50	± 20	± 20	± 10	± 20
RE6	81.93	32.17	± 50	± 100	± 50	± 50	± 20	± 50	± 10	± 20
RE7	163.4	64.16	± 1.0	± 500	± 1.0	± 200	± 50	± 100	± 50	± 100
RE8	325.7	127.9	± 1.0	± 500	± 1.0	± 200	± 1.0	± 200	± 50	± 100
RE9	644.9	253.2	± 5.0	± 1000	± 2.0	± 500	± 2.0	± 500	± 1.0	± 200
RE10	1275	500.8	± 5.0	± 1000	± 2.0	± 500	± 2.0	± 500	± 1.0	± 200

*Absolute tolerance on RE1.

TABLE IB.
SUMMING RESISTOR TABLE CORRESPONDING TO IA. VALUES.

		6 Bit $\pm 1/2$ Bit Array Error = $\pm .8\%$ Error Allocated to Resistors = .16%				7 Bit $\pm 1/2$ Bit Array Error = $\pm .4\%$ Error Allocated to Resistors = .08%				8 Bit $\pm 1/2$ Bit Array Error = $\pm .2\%$ Error Allocated to Resistors = 400 ppm				9 Bit $\pm 1/2$ Bit Array Error = $\pm .1\%$ Error Allocated to Resistors = 200 ppm			
V Full-Scale	Resistor No.	Nominal Resistance k Ω	Nominal R/R E1 Ratio	Ratio Tolerance at 25°C	T.C. max (-20°C -85°C) of Resistor Ratios ppm/°C	Nominal Resistance k Ω	Nominal R/R E1 Ratio	Ratio Tolerance at 25°C	T.C. max (-20°C -85°C) of Resistor Ratios ppm/°C	Nominal Resistance k Ω	Nominal R/R E1 Ratio	Ratio Tolerance at 25°C	T.C. max (-20°C -85°C) of Resistor Ratios ppm/°C	Nominal Resistance k Ω	Nominal R/R E1 Ratio	Ratio Tolerance at 25°C	T.C. max (-20°C -85°C) of Resistor Ratios ppm/°C
5 V	R S1 R S2	1.650 0	.648 ----	$\pm .50$ ----	± 20 ----	1.780 0	.698 ----	$\pm .50$ ----	± 5 ----	1.840 .068	.723 .0267	$\pm .50$ ± 1.0	± 2 ± 20	1.885 .068	.740 .0267	± 10 ± 1.0	± 2 ± 20
10 V	R S1 R S2	3.300 0	1.295 ----	$\pm .50$ ----	± 20 ----	3.560 0	1.395 ----	$\pm .50$ ----	± 5 ----	3.680 .130	1.445 .0510	$\pm .50$ ± 1.0	± 2 ± 20	3.770 .130	1.480 .0510	± 10 ± 1.0	± 2 ± 20

TABLE IC.
R_S' (POT.) RESISTANCE VALUES CORRESPONDING TO IA. AND IB. VALUES

6 Bit $\pm 1/2$ Bit Array Error = $\pm .8\%$ Error Allocated to Resistors = .16%					7 Bit $\pm 1/2$ Bit Array Error = $\pm .4\%$ Error Allocated to Resistors = .08%				8 Bit $\pm 1/2$ Bit Array Error = $\pm .2\%$ Error Allocated to Resistors = 400 ppm				9 Bit $\pm 1/2$ Bit Array Error = $\pm .1\%$ Error Allocated to Resistors = 200 ppm			
V Full-Scale	Nominal Resistance k Ω	Resistance Tolerance	Resolution Ω	T.C. max ppm/ $^{\circ}\text{C}$	Nominal Resistance k Ω	Resistance Tolerance	Resolution Ω	T.C. max ppm/ $^{\circ}\text{C}$	Nominal Resistance k Ω	Resistance Tolerance	Resolution Ω	T.C. max ppm/ $^{\circ}\text{C}$	Nominal Resistance k Ω	Resistance Tolerance	Resolution Ω	T.C. max ppm/ $^{\circ}\text{C}$
5V	1.000	$\pm 5\%$	1.3	± 50	.500	$\pm 5\%$	1.3	± 20	200	$\pm 5\%$	.636	± 20	100	$\pm 5\%$	.431	± 20
10V	1.500	$\pm 5\%$	2.6	± 50	1.000	$\pm 5\%$	2.6	± 20	500	$\pm 5\%$	1.731	± 20	200	$\pm 5\%$	.636	± 20

If greater accuracy over a restricted temperature range is required, then each emitter resistor may be individually trimmed. Using the nominal resistor ratios of Table I and allowing for $\pm 0.1\%$ adjustment, the nonlinearity errors due to manufacturing mismatches in the $\mu A722$ may be trimmed out at a given temperature. The accuracy of the converter will then be due primarily to the temperature coefficient of the full-scale current, which has the typical characteristics shown in Figure 4.

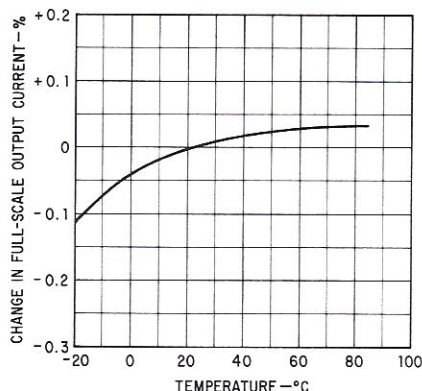


Fig. 4. Typical full-scale output current as a function of ambient temperature.

Basic Digital-to-Voltage Conversion

Normally, a voltage proportional to the input code is required, and an operational amplifier operating in the inverting mode provides the conversion from current to voltage. Figure 5 shows the connection. From basic operational amplifier theory, the output voltage is simply:

$$E_{OUT} = I_S R_S \text{ where } R_S = R_{S1} + R_{S2} + R'_S \quad (2)$$

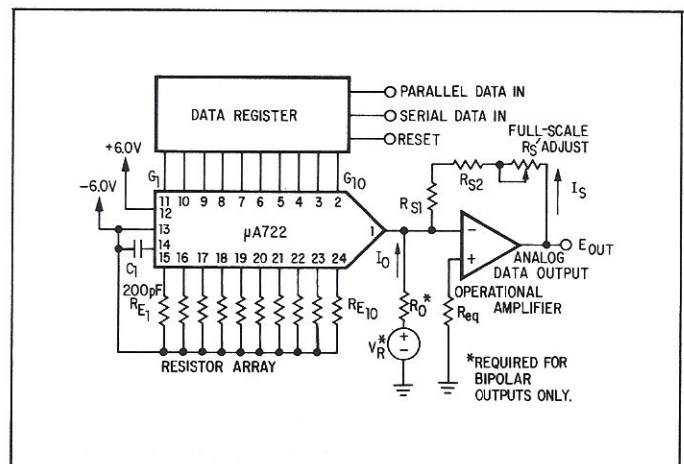


Fig. 5. Typical digital-to-analog converter.

Selection of Summing Resistors

Summing resistor R_S is selected to give the required output voltage swing (usually 5 or 10 volts). Since the full-scale output current of the device may range from 2160 to 3000 μA , provision must be made to trim R_S to obtain the exact output voltage swing. For good ratio tracking with temperature, R_S must track R_{E1} more closely than the capability of most potentiometers. Hence, two fixed series resistors, R_{S1} and R_{S2} , are given in Table I to permit adjustment over the full current range of the $\mu A722$ (by choice of shorting R_{S2}), and yet permit use of an available potentiometer with TCR considerably worse than that required of R_S .

From Equations (1) and (2), it can be seen that E_{OUT} depends on the ratio of $\frac{R_S}{R_E}$, and therefore batch fabricated resistors with poor absolute value control may be used for the R_{EJ} and R_S .

PERFORMANCE

Accuracy

The factors defining the accuracy of the μ A722 are:

- (1) Full-scale current (I_{FS}) drift with temperature
- (2) Nonlinearity: worst-case deviation at a given temperature from a straight line drawn through zero and I_{FS} (Code 1,1,1...1) at that temperature,
- (3) Error: worst-case deviation from the calibrated straight line (normally at 25°C) value over a specified temperature range.

These concepts are illustrated in Figure 6. The nominal current lines are obtained by joining the zero current and the I_{FS} points. (The nonlinear curve is chosen for illustrative purposes and is not typical for the $\mu A722$). Since, by definition, I_{FS} has zero nonlinearity, a given code and its complement have nonlinearities of equal magnitude but opposite sign.

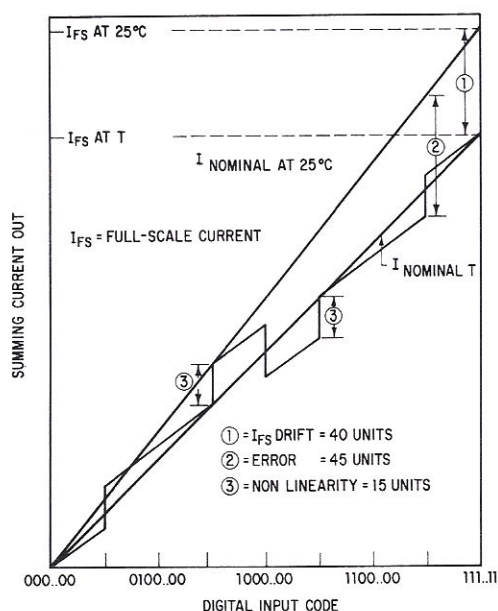


Fig. 6. Hypothetical summing current vs. digital code curve at T to illustrate the concepts of I_{FS} drift, nonlinearity, and error.

The Error is the most significant parameter. For constant temperature operation,

ERROR = NONLINEARITY:

for a unit with zero nonlinearity,

$$\text{ERROR} = I_{\text{FS}} \text{ DRIFT.}$$

For all other cases,

$$I_{\text{ES DRIFT}} \leq \text{ERROR} < I_{\text{ES DRIFT}} + \text{NONLINEARITY}$$

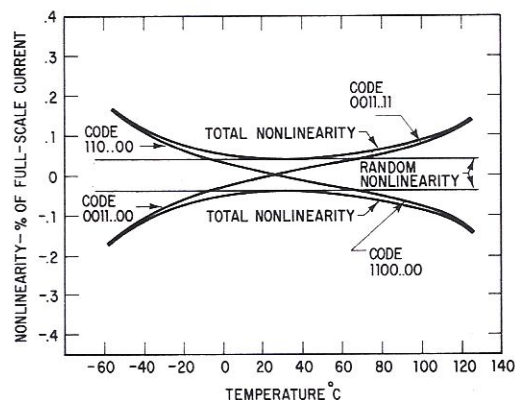
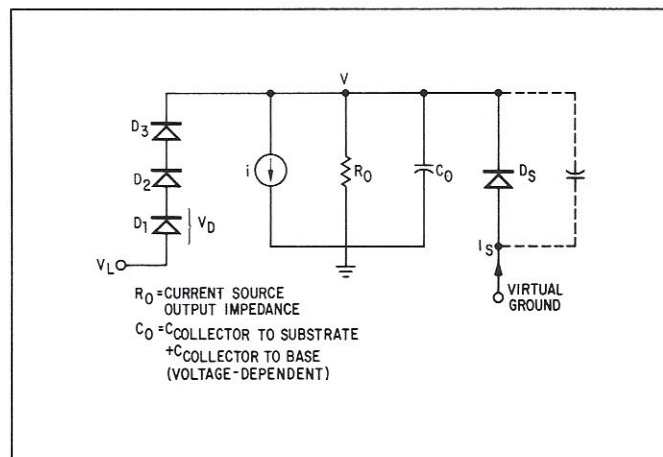


Fig. 7. Nonlinearity vs. temperature: typical graphs.

The nonlinearity of the μ A722 is composed of two components, as shown in Figure 7. One is random, and the other is temperature- and code-correlated. At room temperature, the μ A722 can have zero nonlinearity through trimming of the individual R_{E_j} . If nominal values of the R_{E_j} 's are used, nonlinearity appearing at 25°C will be random in nature.

Speed

The speed of the $\mu A722$ is defined as the settling time after switching to within one-half of the least significant bit value. A simplified diagram of any one of the bit current sources is:



Potential V when V_L is high = $V_{LH} - 3V_D$

when V_L is low $= - \frac{E_{th}}{V_D}$

Therefore, there is a change in V of $V_{LH} - 2V_D$

While this change in V is occurring, both current steering paths are non-conducting. R_O is large, and capacitor C_O provides all the current required by the current source. The time required for this change in voltage is

$$\Delta t \approx \frac{V(\Delta C_O) + C_O(\Delta V)}{i} \approx \frac{C_O(V_{LH} - 2V_D)}{i} - \frac{V(\Delta C_O)}{i} \quad (3)$$

For a constant V_{LH} , switching time is inversely proportional to current; i.e., it will be limited by the least significant bit.

To turn on I_S , V has to change $V_{LH} - 2V_D$; to turn it off, V has to increase approximately 100 mV from $-V_D$. Since normally $V_{LH} - 2V_D > 100$ mV, the turn-on time determines the maximum speed.

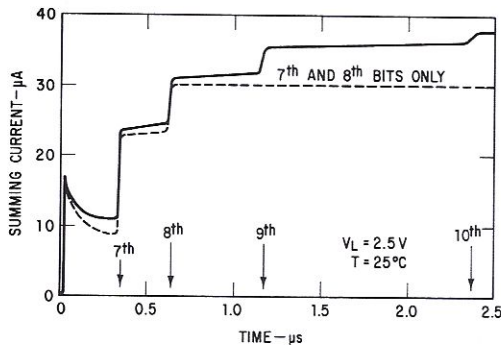


Fig. 8. Turn-on time of 7th, 8th, 9th, and 10th bits.

Figure 8 shows the current waveform obtained after switching bits 7, 8, 9, and 10. The current spike at 30 nsec is due to the capacitive feedthrough from the logic inputs to the summing current terminal. Only a very small fraction of this is feedthrough along D_1 , D_2 , D_3 , and D_5 ; most of it is due to capacitance associated with the package and external connections. There is a current flow of 11 μA before the 7th bit turns on (< 350 nsec). This is due to the voltage changing across the capacitance of D_S as V varies.

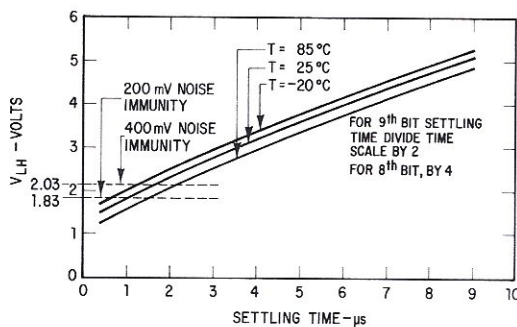


Fig. 9. Settling time - 10th bit.

From equation (3), settling time is proportional to $V_{LH} - 2V_D$; consequently, it will be a strong function of the high logic level and temperature (through V_D). Figure 9 illustrates that with $V_{LH} = 1.90$ V, the $\mu A722$ has at least 300 mV noise immunity and at most 1.60 μsec speed for 10 bits, 800 nsec for 9 bits, and 400 nsec for 8 bits.

Switching Thresholds

The high logic threshold is the minimum V_{LH} ($V_{LH \min}$) necessary to make $I_S = (1/2) I_{LSB}$; the low logic threshold is the maximum V_{LL} ($V_{LL \max}$) necessary to make $I_S = I_{FS} - (1/2) I_{LSB}$.

These voltages are limited by the first bit according to the equation:

$$V(T) \approx 2V(T)_{BE} \quad \left| \quad I = 300 \mu A \pm \frac{kT}{q} \ln X \right. \quad (4)$$

where $X = 2^N$

N = number of bits used

"+" for $V_{LH \min}$

"-" for $V_{LL \max}$

Table II summarizes the results. The low temperature extreme limits $V_{LH \min}$, while $V_{LL \max}$ is restricted by the highest temperature.

TABLE II.

	LEAST SIGNIFICANT BIT	SWITCHING THRESHOLD AT			ABSOLUTE LIMIT OVER -20°C to +85°C RANGE - VOLTS
		-20°C	+25°C	+85°C	
$V_{LH \min}$	8	1.66	1.45	1.23	1.66
	9	1.64	1.47	1.25	1.64
	10	1.63	1.49	1.27	1.63
$V_{LL \max}$	8	1.36	1.17	.89	.89
	9	1.34	1.15	.87	.87
	10	1.33	1.13	.85	.85

GENERAL INTERFACE REQUIREMENTS

Logic Interface

The $\mu A722$ is compatible with most types of bipolar digital integrated circuits. The guaranteed $\mu A722$ input thresholds of 0.7 V for V_{IL} and 2.1 V for V_{IH} , in conjunction with an extremely high input impedance, allow operation with TT μL , DT μL , LPDT μL , RT μL , LPRT μL , C μL and CT μL families of logic.

Compatible Current Sinking Logic (CCSL) consisting of TT μL , DT μL , LPDT μL , and CCSL Medium Scale Integration Logic have guaranteed worst-case output voltages of $V_{OL} = 0.4$ V, $V_{OH} = 2.5$ V at full fan-out. This allows a $\mu A722$ to be driven with no loss of logic fan-out.

Complementary Transistor Logic (CT μL) inverters, buffers, and flip-flops provide typical output voltages of $V_{OL} = -0.5$ V and $V_{OH} = 2.4$ at low fan-outs, adequate for $\mu A722$ operation.

Current Sourcing Logic such as RT μL , LPRT μL and C μL have output swings on the order of $V_{OL} = 0.4$ V and $V_{OH} = 1.2$ V when operating at full fan-out. This V_{OH} is unacceptable for driving the $\mu A722$; thus, no current sourcing loads may be driven from an output which is driving a $\mu A722$ input unless worst-case analysis determines that the $\mu A722$ V_{IH} threshold will be met.

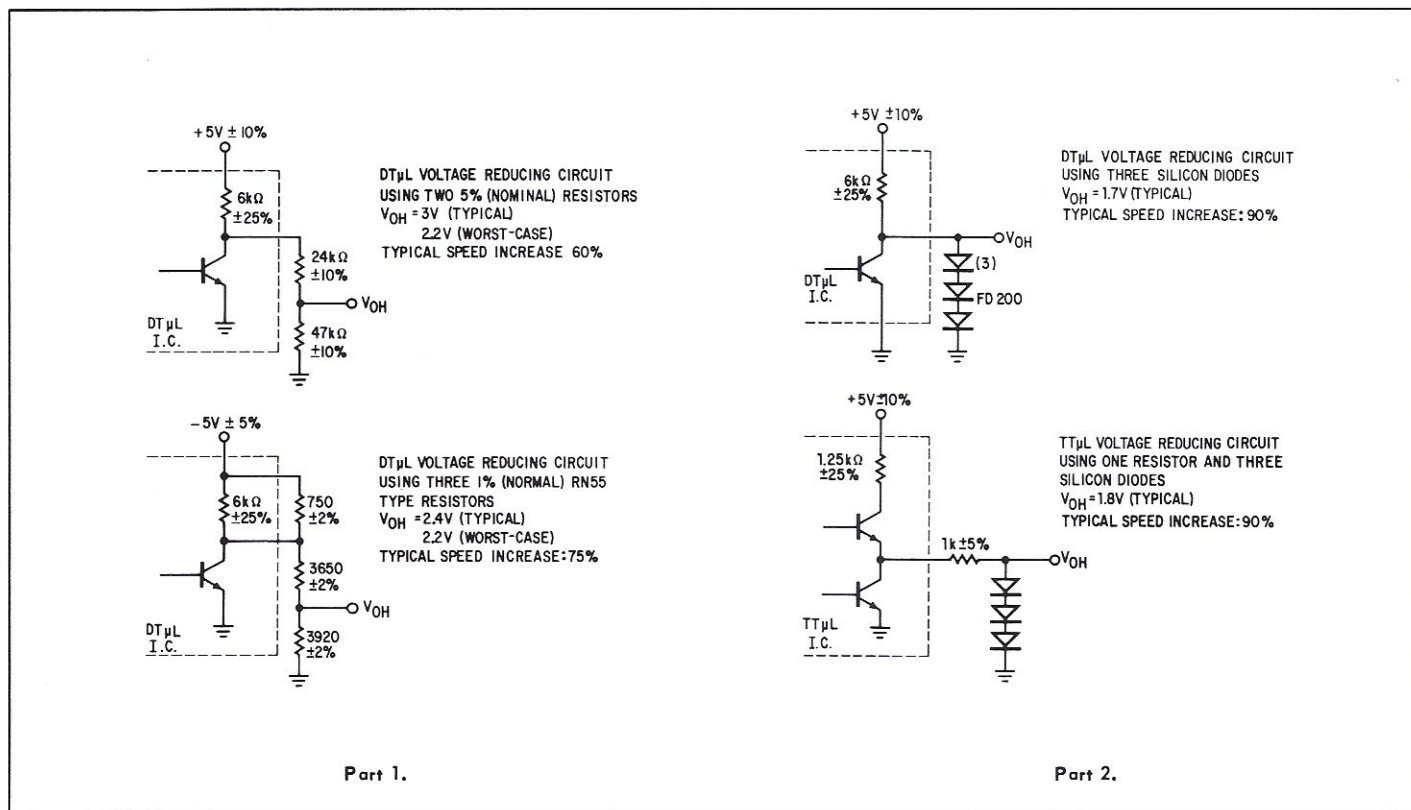


Fig. 10. Representative voltage reducing networks for minimizing $\mu A722$ switching time (for least significant bits).

For maximum speed applications, it is desirable to lower the logic level on the least significant bits. In general, the closer the V_{IH} is to the threshold, the faster the $\mu A722$ will operate. The V_{IH} must, at the same time, maintain an adequate noise margin with worst-case tolerance of power supplies, temperature, and components. Since the $\mu A722$ input threshold is essentially two diode-drops above ground (see Table II for exact value), a technique which will "track" this threshold with temperature will give the fastest operation over a temperature range.

Some representative voltage reducing networks are shown in Figure 10. The diode networks will provide approximately one diode-drop noise immunity. The resistive dividers were calculated for 2.2 V minimum worst-case output.

Current Determining Resistors

Individual current setting resistors are required for each bit used in the $\mu A722$, and a matched feedback resistor for current/voltage conversion. Table I listed the recommended resistor values and temperature coefficients. Tolerances were determined by allocating about 20% of the total 1/2 bit error to resistor imperfection. If trimming is to be done, parallel or series potentiometers may be used, but TC mismatch between the primary resistors and the trimpots must be considered. The greater the TC difference, the less the tolerable trim range for a given required accuracy and temperature range.

Since the current through the resistors is constant, wire-wound resistors having significant inductance may be used for the current setting resistors with no sacrifice in speed. However, the current/voltage converting feedback resistor, which receives the $\mu A722$'s switched current steps, must be non-inductive for

high speed D/A operation. Thus, for high speed operation, two constraints are placed on the combination of current setting resistors and feedback resistor. First, their TC's must track; second, the feedback resistor must have low inductance. If TC tracking rather than very low TC is relied on to meet accuracy requirements, a third constraint must be considered: the need for a low R_{TH} , or thermal resistance, between the feedback resistor and the others. The reason is that the temperature of the feedback resistor will vary from ambient as the square of I_S , the $\mu A722$ summing current, averaged over the feedback resistor's thermal time constant. For a 0 to 5 V encoder, the maximum power dissipated is $(2.5 \text{ mA})^2 \times 2 \text{ k}\Omega$, or 12.5 mW. This causes less than 1°C rise in many discrete component resistors, but can be significant for miniature film resistors unless they have low TC.

Power Supplies, Noise, and $\mu A722$ Stability

The $\mu A722$ has at least 20:1 built-in V^+/V^- power supply rejection* at DC, and even greater rejection can be established at higher frequencies by use of a large stabilization capacitor (say .01 μF). However, high frequency variation of the V^- supply relative to ground will produce AC error current on the summing line via the capacitance between the $\mu A722$'s substrate and output line. It should be emphasized that such error currents may be innocuous in low speed applications where some form of integration follows D/A conversion. However, for high speed, high accuracy applications, high frequency noise, up to several MHz,

* For the $\mu A722$, PSR is defined as $\% V^+/V^-$ variation divided by $\% I_{FS}$ variation, or vice versa.

must be controlled. High frequency variation of V^+/V^- , and V^- /ground and/ or I_S can result from several causes:

- (1) Spurious pickup on supply and ground leads.
- (2) Ringing of V^+ and ground leads due to the switching of I_S from V^+ to summing line (or vice-versa).
- (3) Ringing due to inadequate stabilization of the $\mu A722$'s internal regulator.

By applying techniques appropriate to the application, as described in the next several paragraphs, the sources of high frequency error can readily be eliminated or reduced to a level permitting high speed operation of the $\mu A722$ within $10 \text{ bit} \pm 1/2 \text{ bit}$ accuracy (temperature variation not considered).

Principal Load and Power Supply Configuration

The principal load and power supply configurations for application of the $\mu A722$ are expected to be combinations of the following three categories:

- (1) $\mu A722$ drives either:
 - (a) High or low speed inverting op amp (see Fig. 5).
 - (b) Resistive load to ground (see Fig. 11).
- (2) Available power supplies are either:
 - (a) Logic Supply (0 to +6 V) and two analog supplies (0 to +12 V, and 0 to -12 V) or
 - (b) Logic supply (0 to +6 V) and a single, floating analog supply (12 V to 18 V)--i.e., the "minimal supply" case.
- (3) Length of supply and load leads:
 - (a) Short (<3")
 - (b) Long (>3").

The transimpedance op amp case is expected to be the principal load case, but the supply configuration depends strongly on the user's system. Generalized AC equivalent circuits for the two load cases are given in Figures 1 and 3 of the Appendix.

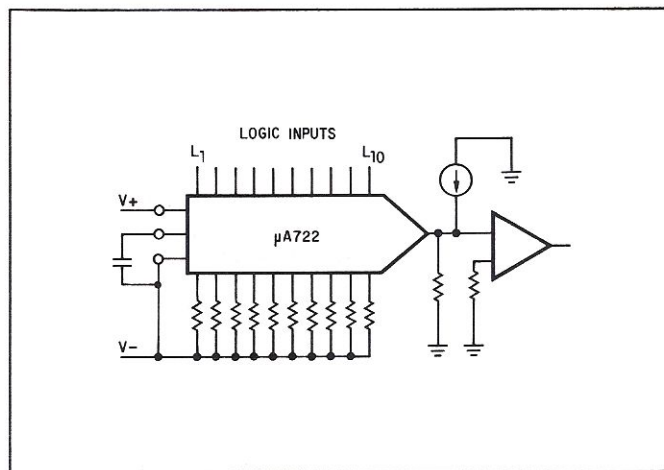
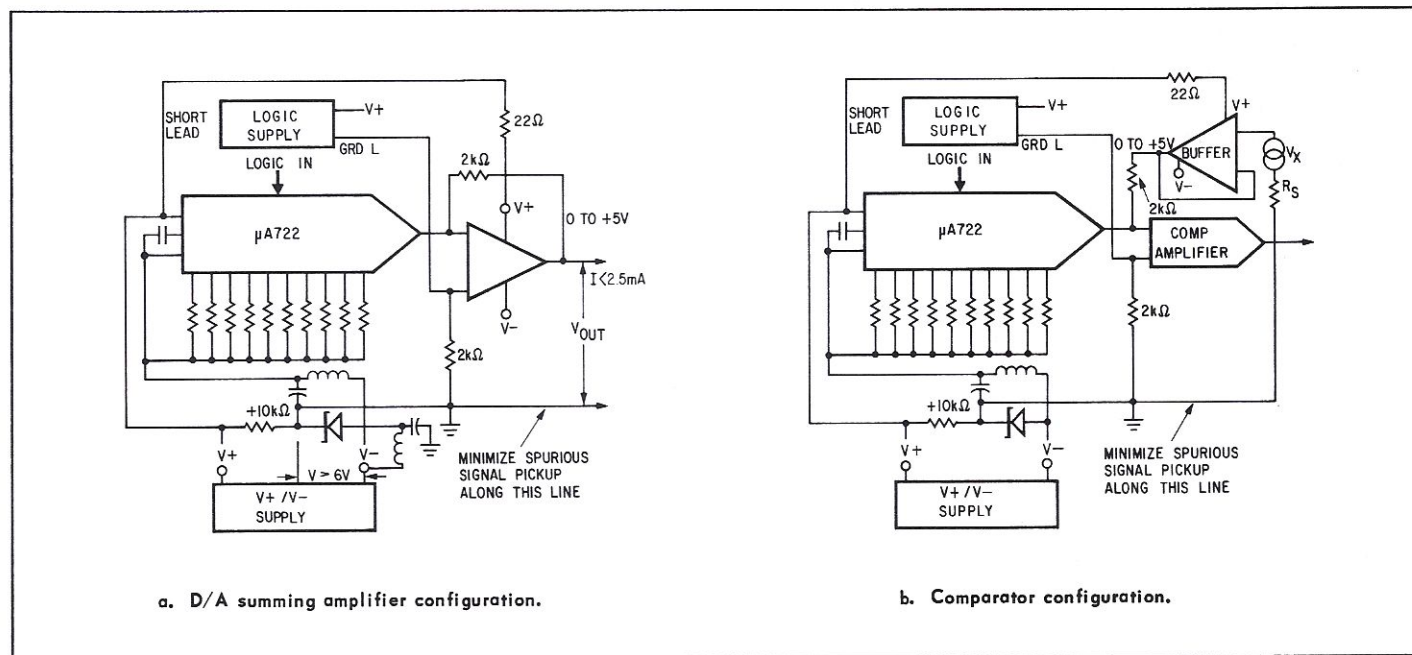


Fig. 11. Connection showing resistive load to ground.

Control of Spurious Pickup

The $\mu A722$ must normally function in proximity to a digital system with high noise-pulse levels on the logic supply and ground leads, and via electromagnetic coupling. Additionally, RFI may be present from nearby subsystems. To control the levels of such spurious signals, it is recommended that a combination of the following techniques be considered, depending on noise levels, and economic, miniaturization, and reliability considerations of a specific application:

- (1) Minimize the effective length of supply and ground leads by locating a dual regulator adjacent to the $\mu A722$.
- (2) Maintain analog ground on a bus wire separate from the digital ground (see Fig. 12).
- (3) Insert an LC filter into the V^- supply path adjacent to the $\mu A722$, with a cutoff frequency <100 kHz.



a. D/A summing amplifier configuration.

b. Comparator configuration.

Fig. 12. Schematics of supply lead problems related to the 2.5 mA step between all "1's" and all "0's" codes. In both cases, (1) use of a common V^+ for $\mu A722$ and signal I/O amplifiers is recommended and (2) minimum ground pickup must be maintained between amplifier input reference and external signal ground.

Stabilization and Filtering of the $\mu A722$ Internal Regulator

The $\mu A722$ internal regulator will normally oscillate unless a capacitor is placed between its stabilization terminal and V^- . As little as 3 pF may stabilize a specific unit (e.g., stray capacitance) but its response to supply transients, such as that resulting from a code change into the $\mu A722$, may be underdamped. This is illustrated in Figure 13, where a set of approximate power supply rejection versus frequency curves is given for various values of stabilization capacitance. Normally 1000 pF $\lesssim C$ is recommended. If miniaturization is a problem use $C = 200$ pF.

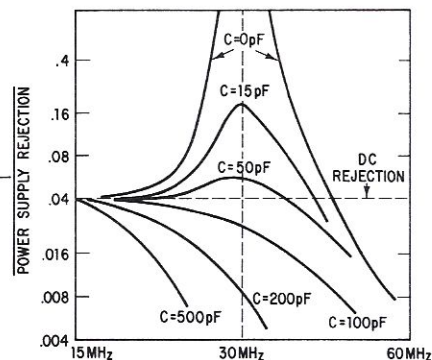


Fig. 13. $\mu A722$ power supply response to spurious sinusoidal components between V^+ and V^- , as a function of stabilization capacitance.

Control of Lead Ringing from $\mu A722$ Switching

The presence of lead inductance in conjunction with collector-to-substrate capacitances of the $\mu A722$ establishes an LC network which can ring when the $\mu A722$ switches. The impact of such ringing depends partly on the supply rejection of the $\mu A722$, and partly on the integrating properties of the D/A load. The former was seen in the previous paragraph to depend on the value of stabilization capacitance. The problem of reducing the ringing amplitude is analyzed in the Appendix for both resistive and op amp loads, where essentially the following principles are derived:

For the op amp load (see Appendix Fig. 3 & 4 for symbol definitions)

$$V^+(t) - V^-(t) \approx 2.5 \text{ mA} \sqrt{\frac{L}{C_1}} e^{-\frac{t}{2R_1C_1}} \sin \frac{t}{\sqrt{LC_1}} \quad (5)$$

where $L = L_+ + L_-$.

Both discrete and monolithic high slewing rate op amps have lower high frequency power supply rejection than the $\mu A722$, and therefore ringing of the op amp V^+ may have to be reduced despite adequate ringing rejection by the $\mu A722$. A convenient and effective damping method is to insert a small resistor (r) in series with the op amp V^+ (see Fig. 12). The damping time constant is then dominated by $\tau = \frac{2L}{r}$ instead of R_1C_1 in Eq. 5, and should be made small enough to assure that the ringing envelope is damped below the necessary error level within the required D/A response time. The maximum value of r is limited by its effect on DC regulation with switching of $0 \leq I_S \leq 2.5 \text{ mA}$. This effect can be minimized by using a common V^+/V^- supply for both $\mu A722$

and transimpedance op amp so that current traversing the $\mu A722$ current sources comes either directly from V^+ , or from V^+ via the op amp output stage into the $\mu A722$ summing line. Experience has shown that for this supply configuration, $r = 22\Omega$ is effective for a 10-bit D/A with supply leads up to 3 to 4 feet long.

Recommended Supply and Lead Configurations

Two generic configurations are recommended, one for an op amp sourcing the summing current and the second for a low resistance ($\leq 200\Omega$) source from summing line to ground (as might be used for a current-encoding A/D).

Configuration I is the more important. It is shown schematically in Figure 12. Note that most of the techniques previously discussed in this section are combined in it to give best performance. Some may be dropped for simplicity in specific applications. These techniques are:

- (1) Use of an analog ground wire tied to digital ground at only one point, so that no digital signals flow in it.
- (2) Minimum line length containing the V^+ current transient by connecting the $\mu A722$ directly to V^+ , and branch feeding the amplifier with a short lead.
- (3) Light loading of the D/A buffer op amp.
- (4) LC filtering of V^- .
- (5) ($r < 50\Omega$) damping resistor in V^+ line.

In addition, a most important technique, not previously mentioned, is the use of a nearly floating, single analog supply referenced to digital ground by a low-cost zener diode, such as the reverse E-B junction of a transistor. This is made possible by the fact that just 30 μA (about 3 μA per logic input) must be returned to the logic supply from the $\mu A722$'s V^- current.

For the system already having separate V^+ and V^- supplies, or when high supply levels are needed by the op amp, it is recommended that the above common-supply techniques be retained by use of zener dropping diodes from the op amp supply levels, to supply the $\mu A722$ at +6 V.

The recommended configuration is believed to provide the best compromise between cost, complexity, and performance. If performance is the dominant consideration, separate $\mu A723$ V^+ and V^- regulators* are recommended. An example circuit is given in Figure 14.

Configuration II is shown schematically in Figure 15. Since for this case the I_S step switches between two separate leads, V^+ and V^- ground, it is recommended that:

- (1) The V^+/V^- ground/summing-reference lead triangle be composed of physically short leads, and that they be physically close and parallel for inductance cancellation as shown in Figure 15.
- (2) The V^+ lead must be physically short to minimize inductance.
- (3) A damping RC be connected between V^- and the summing reference (signal ground).

* Also see the $\mu A723$ Application Note "A Monolithic Voltage Regulator", by D. Lieux.

Values on the order of 50Ω and $C \geq 1000\text{ pF}$ should be used, and these components should be checked for fidelity of their characteristics at frequencies up to 30 MHz.

- (4) Inductive filtering of V^- (using the damping RC as an AC shunt load) be used.

- (5) ($r < 50\Omega$) damping resistor be placed in V^+ line.

Again, best performance can be achieved with separate V^+ and V^- regulators, but at added cost and component count.

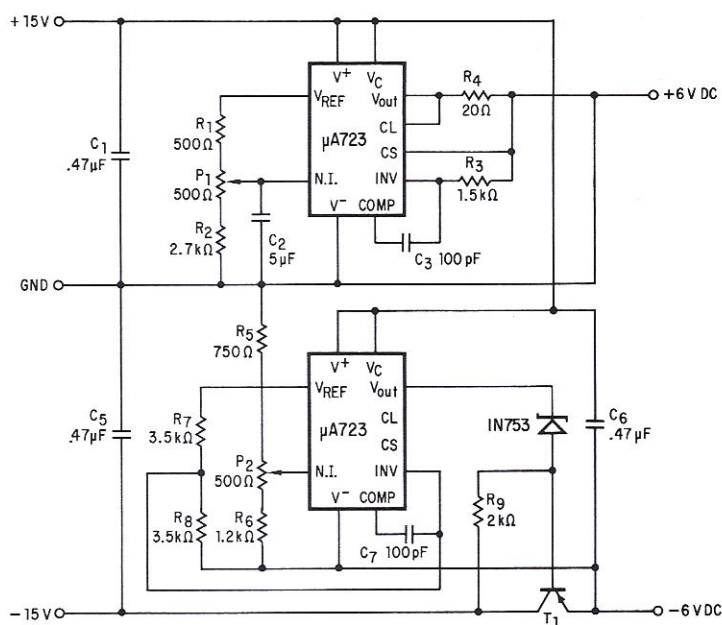


Fig. 14. $\pm$ Regulator for best $\mu A722$ performance (it is normally unnecessary).

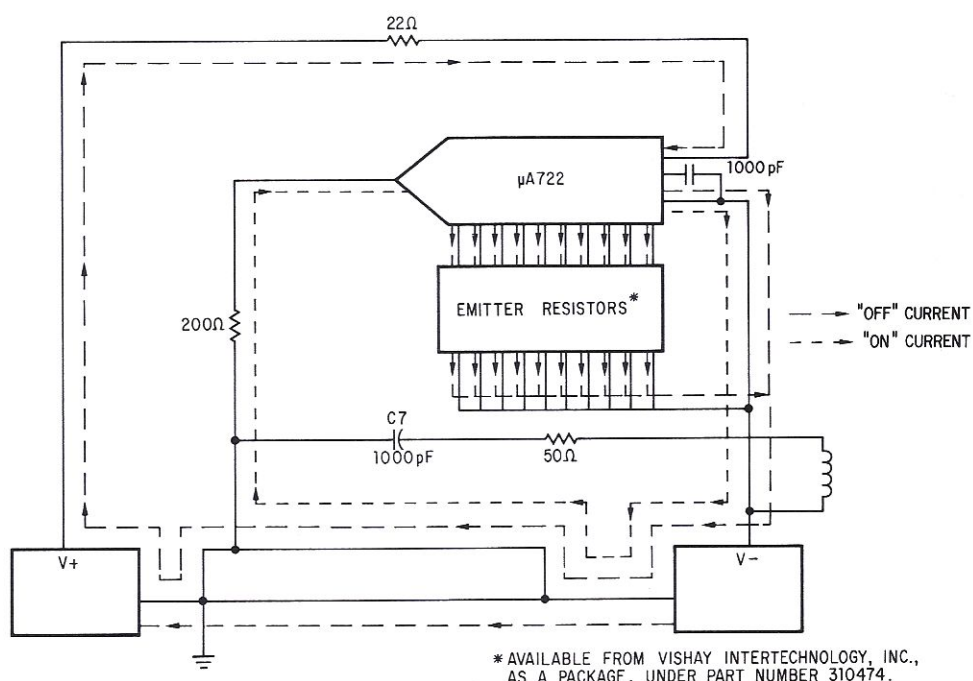


Fig. 15. Recommended ground damping, and filtering configuration for $\mu A722$ with grounded resistive source.

Failure Modes

Various types of misuse of the $\mu A722$ will result in excess current in a junction or connecting metal, and permanent damage. Supply limiting will save the unit in some cases. The time and current levels necessary for permanent damage are not presently known. Only simple application errors, involving a single type of discrepancy, have been considered. Multiple erroneous connections, except those induced by package symmetry, have been ignored.

A brief description of potential ways to misuse the $\mu A722$, and their effects, follows. The symbol "i" in various subscripts refers to the general, i^{th} bit.

Erroneous Insertion of Unit

- (1) Package inserted upside down

Pin 12 is interchanged with pin 13; i.e., V^+ interchanged with $V^- \rightarrow 2V$ forward bias on isolation-collector junctions of Q_{1i} and Q_{2i} .

Total current is divided evenly (approximately) among 20 transistors. Therefore, if power supply current is not limited to about 250 mA, failure will occur.

- (2) Package rotated 180°

Pin 13 is interchanged with pin 1; i.e., collector bias on D_1 to $D_{10} = V^-$; substrate is nominally at 0 V via the external summing line resistor, R_S .

Therefore, V forward bias appears on isolation-collector junctions of D_1 to D_{10} , but limited current is available through R_S , and failure will not occur. However, in applications in which the $\mu A722$ drives a low resistance to ground, such as a meter movement, the current could reach damage levels.

Exceeding Maximum Logic Levels

- (1) $V_{\text{logic}} > 6.8V$ for $V^+ = 6V$
 Q_{1i} CB junctions forward-biased -- unlimited current.
- (2) $V_{\text{logic}} > 8.0V$ for $V^+ > 7.2V$
EB junctions are broken down, and unlimited current through the Q_{1i} , D_{1i} , Q_{2i} , D_i chain.

Since it is possible that only one or two of the logic drivers exceed the maximum level, current limiting of power supplies will not work.

Shorting Various Combinations of the 24 Leads

- (1) Short pin 1 to pin 13; current summing bar to V^-
If any of the logic inputs $> 2.5V$, then D_i EB junction is broken down, large current flows through the Q_{1i} , D_{1i} , Q_{2i} , D_i chain.
- (2) V^+ shorted to ground
 V_L forward bias appears at CB junctions of Q_{1i} .

Reversal of Power Connections

- (1) Complete reversal is covered under "erroneous insertion (1)".
- (2) V^- supply tied to V^+ terminal

Forward-biased Q_{1i} CB junctions into the external logic terminals, and very large currents can flow depending on logic output current capacity.

II. D/A-A/D CONVERSION AND OTHER SUBSYSTEM APPLICATIONS OF THE $\mu A722$

DIGITAL-TO-ANALOG CONVERTERS

Low Speed Digital-to-Current Conversion

When a current-operated device such as a strip-chart recorder, meter, or deflection coil is to be driven, no operational amplifier is required. The digital-to-analog meter of Figure 16 illustrates this point. A standard 1 mA meter is driven directly from the $\mu A722$. Potentiometer R_p provides a full-scale adjustment by bypassing excess output current. Since analog meters are normally readable to no better than 1%, only a 7-bit input is specified; the unused inputs should be tied to the logic V^+ .

The resistor array is made up of 7 resistors: 4 standard value 1% RN55 types, two standard $\pm 5\%$ carbon composition, and one special value .5% unit. The simplicity and small size of the circuit allows the complete digital-to-analog converter to be mounted within, or on the back of, a meter.

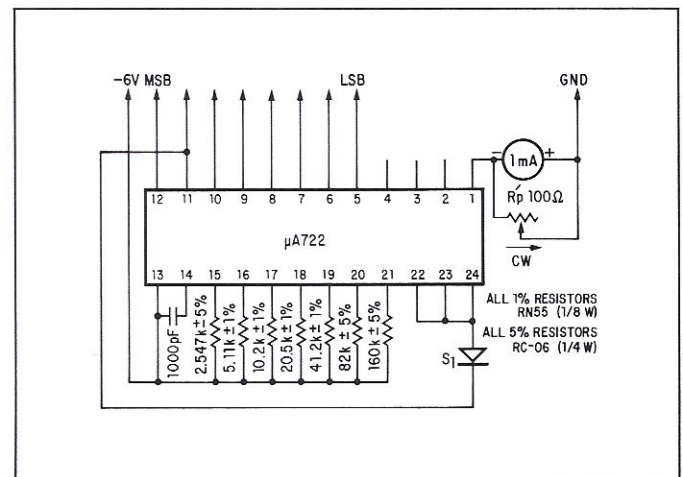


Fig. 16. Digital input meter.

Basic Digital-to-Voltage Conversion with the $\mu A722$

If a voltage proportional to the input code is required, an operational amplifier operating in the inverted mode provides the conversion from current to voltage. Figure 5 showed the basic connection.

Operational amplifiers may require a method of nulling out offset currents and voltages, but normally offsets of high quality discrete and IC amplifiers (e.g., $\mu A709$) are negligible for 10-bit operation with the $\mu A722$.

If the full 10-bit digital input is not required, unused inputs should be tied to the logic power supply.

The $\mu A722$ sinks no output current I_S when all digital inputs are high ($\geq 2.5V$), and maximum current when all inputs are low ($\leq 0.5V$). After inversion by the inverting amplifier, this results in a DAC in which all inputs high result in the most negative voltage output; all inputs low, the most positive. For unipolar outputs, the binary inputs should be connected in complemented form to obtain the desired input code to output relationship. The complemented inputs may be easily obtained from a flip-flop holding register by connecting the $\bar{Q}$ outputs to the $\mu A722$.

Bipolar Outputs

Since the $\mu A722$ acts as a current sink, the operational amplifier output voltage will always be positive or zero. For bipolar or negative voltage outputs, a unity gain inverting amplifier may be switched in, or a positive current I_O may be introduced at the summing point to offset E_{OUT} in the negative direction. The latter case will be described first.

If a highly stable positive voltage V_R is connected through stable resistor R_O , the output voltage is then:

$$E_{OUT} = \left(I_S - \frac{V_R}{R_O} \right) R_S \quad (6)$$

Since full-scale I_S will vary from nominal, provision must be made to trim I_O a similar amount. By thus biasing the amplifier input so that zero is shifted to half-scale, logic transformation of the input code can give bipolar output (as described later). To eliminate errors due to the operational amplifier input bias currents, both input terminals should "see" equal resistances. The $\mu A722$ typically has 1.2 M Ω output impedance; therefore:

$$R_{eq} \approx \frac{R_S R_O}{R_S + R_O} \quad (7)$$

If no offset resistor (R_O) is required, $R_{eq} = R_S$.

As a result of the current source characteristics of the $\mu A722$, the amplifier gain may be assumed equal to unity ($R_{IN} = R_S$) for all practical values of R_S . This has the desirable property of making amplifier frequency compensation independent of output voltage swing.

For bipolar outputs, one of three codes is normally specified. If the DAC is being used with a digital computer, negative numbers will normally be specified in one or two's complement form. For ease of manual inputs, absolute value plus sign may be the most convenient. Table III summarizes these common bipolar codes along with the "natural" $\mu A722$ code. In addition, a $\mu A722$ code is shown for a resistor array with a modified R_1 resistor. Using this table, proper input connections for these codes are easily obtained.

One's complement input code requires the complementing of all digital inputs except the sign bit, and use of the modified R_1 resistor value. Two's complement code again requires complementing all digital inputs except the sign bit. The standard R_1 value is used.

The procedure for absolute magnitude plus sign code conversion may be seen by inspection of Table III. All inputs but the sign bit must be complemented when the sign bit is low, and transmitted in true form when the sign bit is high. Modified R_1 is used. A typical TTL implementation of the required logic is shown in Figure 17, but any logic family may be used.

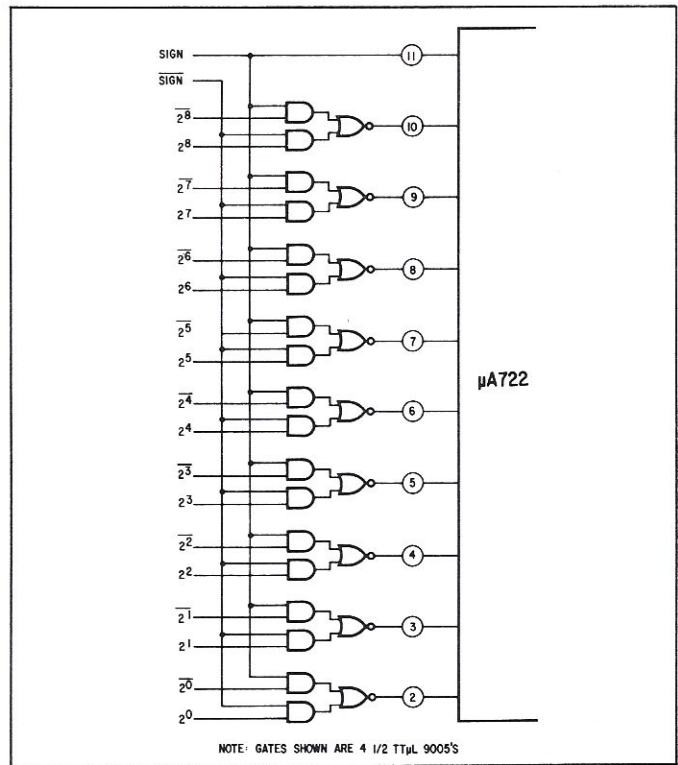


Fig. 17. Absolute magnitude plus sign 10-bit DAC logic.

The modified value of R_1 , used for one's complement and absolute magnitude plus sign codes, is required to decrease the current contribution of the sign bit by an amount equal to the least significant bit. In other words, R_1 must be increased so that $I_1 = I_2 + I_3 + \dots + I_n$, where n is the number of bits in the code, thus shifting zero to exactly half-scale of the $\mu A722$.

Since the change of R_1 will be small, a simple linear relationship may be assumed between R_1 and I_1 so that:

$$R_{1\text{mod}} = \left(\frac{I_1}{I_1 - I_n} \right) R_1 \quad (8)$$

TABLE III.
SUMMARY OF 10-BIT BINARY BIPOLAR CODES
L = ≤ 0.5 VOLTS H = ≥ 2.1 VOLTS

	$\mu A722$ DAC BINARY WEIGHTED RESISTOR ARRAY		$\mu A722$ DAC MODIFIED R_1		ONE'S COMPLEMENT		TWO'S COMPLEMENT		ABSOLUTE VALUE PLUS SIGN	
	MSB	LSB	MSB	LSB	Sign	LSB	Sign	LSB	Sign	LSB
PLUS FULL-SCALE	L	L	L	L	L	H	L	H	L	H
PLUS ONE	L	H	L	H	L	L	L	L	L	L
PLUS ZERO	L	H	L	H	L	L	L	L	L	L
MINUS ZERO	L	H	L	H	L	L	L	L	L	L
MINUS ONE	H	L	H	L	H	H	H	H	H	H
MINUS FULL-SCALE	H	H	H	H	H	L	H	L	H	H

TABLE IVA.
FIXED RESISTOR VALUES FOR THREE-PLACE BCD RESISTOR ARRAYS

Resistor No.	Bit Value	8 Bit $\pm 1/2$ Bit Unit Error Allocated to Resistors = 400 ppm				9 Bit $\pm 1/2$ Bit Unit Error Allocated to Resistors = 400 ppm			
		Nominal Resistance Value k Ω	Nominal Resistance Ratio R/R _{E1}	Ratio Tolerance at 25°C %	T.C. max (-20°C - 85°C) of resistor ratio ppm/°C	Nominal Resistance Value k Ω	Nominal Resistance Ratio R/R _{E1}	Ratio Tolerance at 25°C %	T.C. max (-20°C - 85°C) of resistor ratio ppm/°C
R _{E1}	2.00	2.547	1.000	$\pm 10.0^*$	± 20	2.547	1.000	$\pm 10.0^*$	± 20
R _{E2}	1.00	5.094	2.000	$\pm .02$	± 5	5.094	2.000	$\pm .01$	± 2
R _{E3}	.80	6.379	2.504	$\pm .02$	± 5	6.379	2.504	$\pm .01$	± 2
R _{E4}	.40	12.83	5.036	$\pm .05$	± 10	12.83	5.036	$\pm .02$	± 5
R _{E5}	.20	25.80	10.13	$\pm .10$	± 20	25.80	10.13	$\pm .05$	± 10
R _{E6}	.10	51.03	20.03	$\pm .20$	± 50	51.03	20.03	$\pm .10$	± 20
R _{E7}	.08	63.36	24.88	$\pm .50$	± 100	63.36	24.88	$\pm .20$	± 50
R _{E8}	.04	126.3	49.57	± 1.0	± 200	126.3	49.57	$\pm .50$	± 100
R _{E9}	.02	250.1	98.17	± 1.0	± 200	250.1	98.17	$\pm .50$	± 100
R _{E10}	.01	495.0	194.3	± 2.0	± 500	495.0	194.3	± 1.0	± 200
R _S 5V Full-Scale		1.590	.624	$\pm .50$	± 2	1.630	.640	$\pm .10$	± 2
R _S 10V Full-Scale		3.180	1.248	$\pm .50$	± 2	3.260	1.280	$\pm .10$	± 2

* Absolute tolerance on R_{E1}.

TABLE IVB.
R_S (POT.) VALUES FOR THREE-PLACE BCD RESISTOR ARRAYS

V Full-Scale	8 Bit $\pm 1/2$ Bit Unit Error Allocated to Resistors = 400 ppm				9 Bit $\pm 1/2$ Bit Unit Error Allocated to Resistors = 400 ppm			
	Nominal Resistance k Ω	Resistance Tolerance	Resolution Ω	T.C. max ppm/°C	Nominal Resistance k Ω	Resistance Tolerance	Resolution Ω	T.C. max ppm/°C
5V	.200	$\pm 5\%$	.636	± 20	.100	$\pm 5\%$	.431	± 20
10V	.500	$\pm 5\%$	1.731	± 20	.200	$\pm 5\%$	.636	± 20

For example, an 8-bit DAC requiring the modified value would have the following parameters:

$$\begin{aligned}
 I_1 &= 1280 \mu A \\
 I_8 &= 10 \mu A \\
 R_1 &= 2.547 \text{ k}\Omega \\
 R_{1\text{mod}} &= \left[\frac{1280 \mu A}{(1280 - 10 \mu A)} \right] (2.547 \text{ k}) = 2.567 \text{ k}\Omega
 \end{aligned}$$

The modified R₁ might be implemented simply by adding a 20 ohm resistor in series with R₁.

By using a BCD weighted resistor array (see Table IV), the $\mu A722$ may be used to build a 10-bit BCD DAC. The input range will be decimal 000 to 399.

Overall D/A Speed

The delay associated with the conversion of a digital input to a proportional output of specified voltage is a function of the individual speeds of the logic circuit, the $\mu A722$, and the operational amplifier.

In general, digital logic speeds are more than an order of magnitude faster than linear circuits, and their delays may be neglected. The speed of the $\mu A722$ is dependent on the accuracy required. For example, typical speeds are 0.6 μsec for an 8-bit conversion, 2.5 μsec for 10-bit. These speeds are for logic inputs of 0.5 and 2.3 volts. Where high $\mu A722$ speeds are required, voltage reducing networks such as described in the Logic Interface sub-section should be used on the least significant bits.

Overall D/A Accuracy

The overall accuracy of a linear device is a function of many variables; for a digital-to-analog converter, these include accuracy and temperature dependence of the resistor array, $\mu A722$, operational amplifier, feedback resistor, power supplies, and, if used, offset reference voltage and resistor. If high quality com-

ponents are used, the accuracy limiting element will usually be the temperature stability of the $\mu A722$.

With temperature control such as supplied by a small oven, and individual trimming of array resistors, very accurate operation may be obtained. The only inaccuracy for this case is noise, which limits operation to about 13 bits at 1 megabit, and about 15 bits at 63 kilobits.

Generally, the overall DAC conversion rate will be determined by the operational amplifier. While small output excursions may take place rapidly, worst-case output swings of 5, 10 or 20 volts normally account for the largest delays. This is due to the early roll-off in open loop gain of the operational amplifier, caused by compensation networks. For example, the typical slew rate of a $\mu A709$ with unity closed loop gain and recommended compensation is 0.3 volts/ μsec .

High slewing rate operational amplifiers ($\approx 100\text{V}/\mu\text{sec}$) are available from a number of discrete module manufacturers. By actual test, it was found that these commonly have ringing problems when driven by the $\mu A722$ and required to settle to less than $\pm 1/2$ bit in 10 bits. The trouble seems to be a combination of power supply ringing and inadequate rejection of the high ringing frequency--typically 3 MHz. Surprisingly, the criterion of settling to D/A accuracy often placed amplifiers with lower slewing rates at higher position. In fact an experimental integrated operational amplifier with rated slewing rate of 20 V/ μsec outperformed all discrete operational amplifiers tested. Figure 18 illustrates this. Note that the 8th, 9th and 10th bits are shown switching in practically ideal manner, and that (0.1% = 1 cm) no appreciable ringing is observed. The trace width is due to probe noise.

Figure 18 confirms that speeds of .8 μsec , 1.6 μsec and 3.2 μsec are readily achieved for 8, 9 and 10 bits respectively, without logic dividers.

Some Actual Designs

A moderate speed 10-bit binary, unipolar, serial or parallel input DAC is shown in Figure 19.

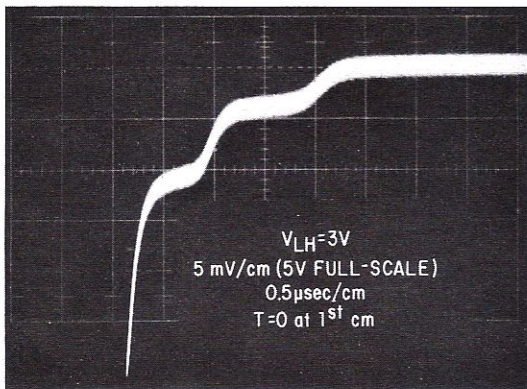


Fig. 18a. $\mu A722$ /experimental op amp switching ON, as it should with typical logic voltage on least significant bits. Note complete absence of ringing.

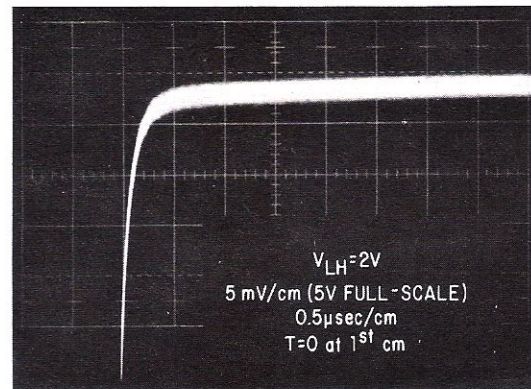


Fig. 18b. $\mu A722$ /experimental op amp switching ON within .05% in 1 μ sec with low V_{LH} . Note complete absence of ringing.

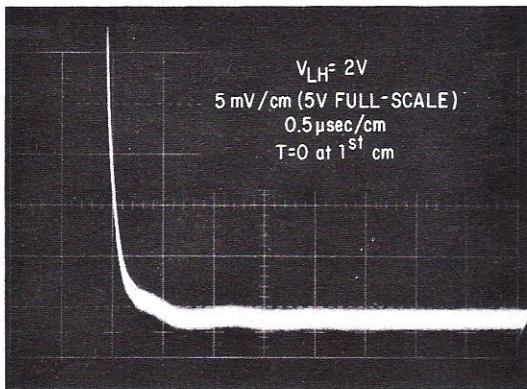


Fig. 18c. $\mu A722$ /experimental op amp switching OFF within .05% in 1 μ sec.

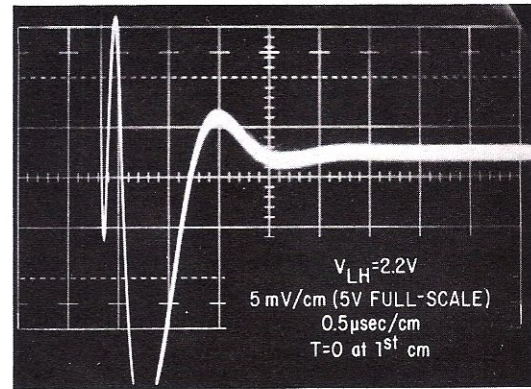


Fig. 18d. $\mu A722$ driving a well-known discrete 100 V/ μ sec op amp. It settles within .05% in 2 μ sec.

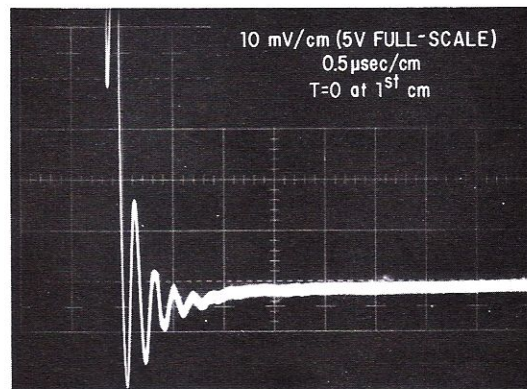


Fig. 18e. A bad example of $\mu A722$ /experimental op amp ringing on turn off due to capacitive loading (mainly from the scope probe with inadequate op amp compensation). Note that it still settles within .05% in 1.5 μ sec.

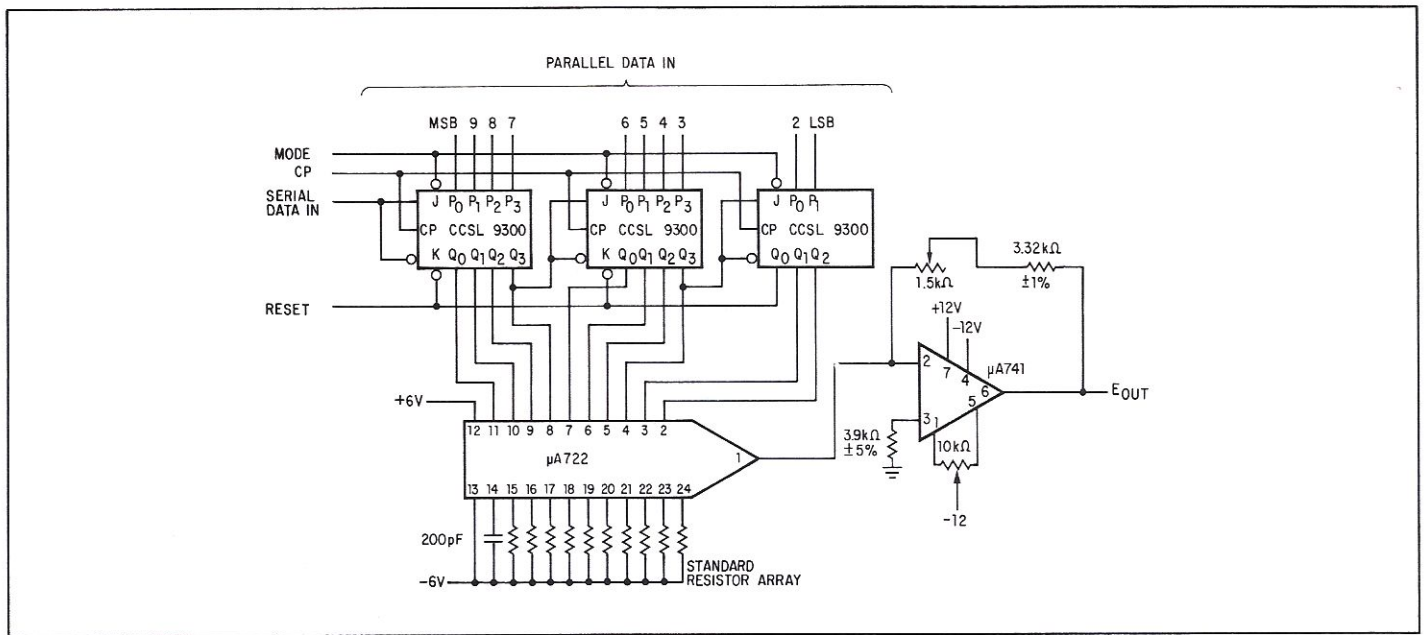


Fig. 19. 10-bit digital-to-analog converter with parallel or serial input.

A holding register of three CCSL 9300 4-bit shift registers provides either parallel input (mode input high) or serial input (mode input low). Both parallel and serial entry are synchronous with the clock.* A parallel asynchronous reset line is provided. The 9300 shift register drives a $\mu A722$ and a standard value resistor array.

A $\mu A741$ integrated circuit operational amplifier is used. For a 0 to +10 V output swing,

$$R_S = \frac{E_O}{I_S} = \frac{10 \text{ V}}{2.56 \text{ mA}} = 3.91 \text{ k}\Omega \quad (9)$$

Since I_S may vary from nominal, a potentiometer having a range of $\pm 5\%$ must be used in series with a fixed resistor to obtain R_S . The nearest standard value is 500 ohms; therefore:

$$R_{S_{\text{FIXED}}} = 3910 - 250 = 3660 \Omega$$

While only $\pm 1\%$ tolerance is required on this resistor, temperature stability must be good. A $\pm 1 \text{ PPM}/^\circ\text{C}$ temperature coefficient was selected.

Measured performance was 26 μsec transition time to 1/2 LSB (5 mV), .01% linearity, and .25% accuracy over the -20 to +85°C range.

A fast 8-bit DAC is shown in Figure 20. The input code is one's complement provided in parallel, and stored in four TT μL 9020 dual flip-flops. The inputs to the $\mu A722$ are taken from the Q output of the sign flip-flop and the Q outputs of the other seven outputs to obtain the one's complement code. Voltage-dropping networks are used on the last three stages to increase $\mu A722$ speed. The unused inputs are returned to +5 volts.

* If a stable D.C. output is required during serial mode input time, a holding register using either 9300's or 9308's should be used.

The resistor array uses a modified value R_1 required for the one's complement code. Since the output is to be ± 5 volts, R_S is chosen for a 10-volt swing while the offset resistor R_0 is chosen to offset the output 5 volts negative. While R_1 and R_0 need only have 1% initial tolerance because of the series potentiometers, they must have good temperature stability. A TC of 1 PPM/ $^\circ\text{C}$ was specified. A high speed discrete component operational amplifier was used to obtain fast transition times from ± 5 volts with output currents up to 18 mA. Measured performance of the complete DAC was a maximum delay time of 2.8 μsec to $\pm 1/2 \text{ LSB}$ ($\sim 20 \text{ mV}$) at room temperature into a 40 pF load.

ANALOG-TO-DIGITAL CONVERTERS

The $\mu A722$ is basically intended for D/A conversion, but it can be used in all forms of A/D conversion as a comparison signal generator. And since A/D converters generally require higher bit rates, the speed of the $\mu A722$ is especially useful in such applications. The principal types of D/A feedback encoders are:

- (1) Staircase counter A/D converter
- (2) Up-down counter A/D converter
- (3) Successive approximation A/D converter

The first two trade high A/D speed for digital simplicity. The latter has the highest random-sample encoding speed, and is presently the most popular configuration because with multiplexing it offers the greatest conversion power per dollar or pound weight.

A staircase converter using a $\mu A722$ can encode to 8 bits in about .25 msec. The up-down counter converter, using the $\mu A722$ and T^2L logic, can easily follow a single signal up to 10 kHz. These techniques may prove the most efficient for local conversion systems, because the counters take less digital circuitry. However, because of its popularity, the successive approximation (SA) configuration was selected for an example application of the $\mu A722$.

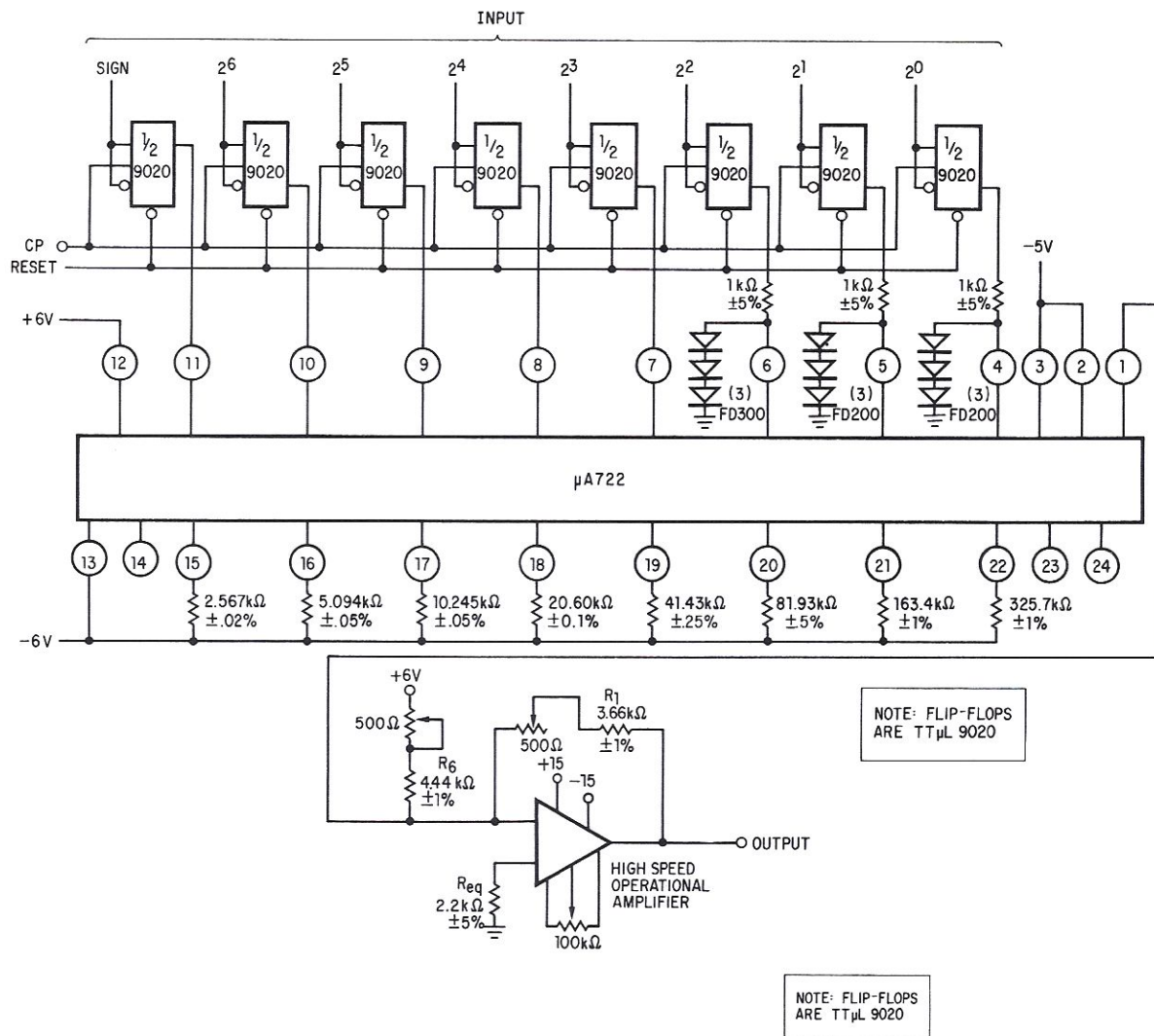


Fig. 20. Fast, 8-bit DAC with one's complement input code. Output is ± 5 V, @ 18 mA.

Successive Approximation Converter

An actual $\mu A722$ SA converter was constructed and tested. The block diagram is shown in Figure 21. It includes a $\mu A722$ D/A converter, a digital programmer and data register block, a comparator, and an input buffer amplifier.

The SA technique is well-known, but for completeness is described for the scheme in Figure 21 as follows:

- (1) A voltage to be encoded, V_X , has subtracted from it a voltage $I_S R_S$ via the summing line resistor R_S ;
- (2) $V_X - I_S R_S$ appearing at the comparator input is compared with 0 V (gnd) by the comparator;

- (3) The digital block successively tries $\mu A722$ bit currents (I_{Si}) starting with the most significant, or largest I_{Si} , and retaining only those bit currents which do not cause the total I_S to pull the comparator input below zero;
- (4) With convergent, arabic codes, such as binary and BCD, the sum of the retained bit currents must approach the condition $I_S R_S = V_X$ within the magnitude of $I_{SLSB} R_S$. Thus with each trial, the I_S "successively approximates" $I_X = V_X / R_S$ closer and closer, and at balance, equals it.

Each block and its interface considerations are discussed in the following paragraphs. Since the $\mu A722$ D/A conversion technique has been presented previously, only the comparator, buffer, and digital block are treated.

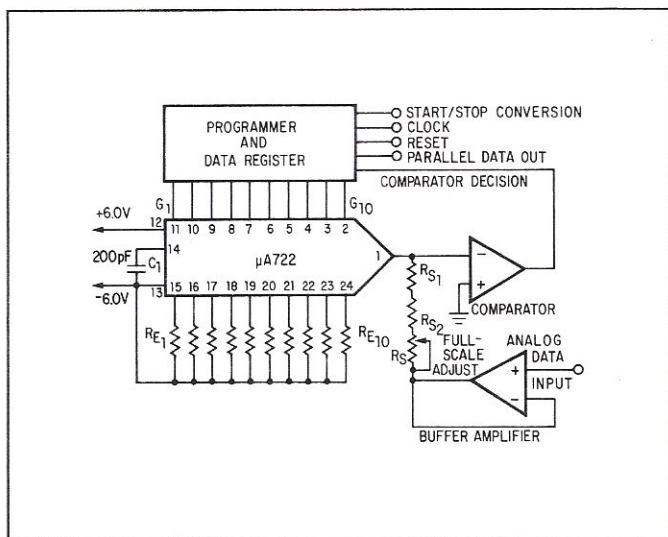


Fig. 21. $\mu A722$ successive approximation analog-to-digital converter.

Input Buffer Amplifier

A unity-gain buffer amplifier is often necessary to remove any effects of input voltage source impedance on the converter accuracy, and is required for source impedances above one ohm when 10-bit converter accuracy is targeted. Obviously its output impedance must be under one ohm. Its speed to settle to within the least significant bit (LSB) should be about one bit period, if it is not to reduce overall conversion rate significantly. A developmental high speed IC operational amplifier capable of 1 μ sec performance was used in the model, and discrete amplifiers of similar performance are available.

Comparator

The comparison amplifier must have three characteristics:

- (1) Be able to resolve the lowest input voltage change $I_{SLSB}R_S$. For 10-bit accuracy and a 5-volt reference, this is .05% of 5 V, or 2.5 mV.
- (2) Draw very low current from the $\mu A722$ summing line. For 10 bits, $I_{SLSB} = 2.5 \mu A$, and therefore the comparator bias offset current should be under 500 nA at minimum temperature.
- (3) Switch in a time which is short compared to the $\mu A722$ switching time.

The $\mu A710$ can handle (1) and (3), but its input bias current is too high to satisfy (2) without a preamp. A single differential stage preamp using the 2N3726 differential pair (Fig. 22) switches in less than 300 nsec. The $\mu A727$ can be used if 1 μ sec switching is adequate.

Digital Programmer and Data Register

This section provides all the necessary digital sequencing, timing and storage to perform the SA control function described

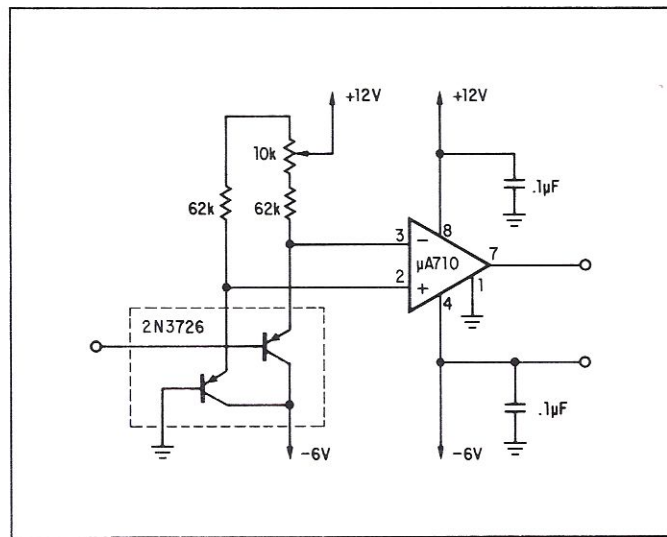


Fig. 22. A/D comparator circuit.

earlier. The logic selected for this example was TT μ L to gain the advantage of the complexity available within this family. In practice, any digital integrated family is acceptable since the switching time of the $\mu A722$ is much slower than all common bipolar integrated logic families.

Sequential control of the bit trials can be done in a number of ways, but shifting a single "1" through a 10-bit program register was selected. A 10-bit data register for storing the answer is obviously required. These two registers account for the majority of the essential digital circuits. The remaining circuits provide the following:

- (1) Flip-flop to store the comparator output.
- (2) Timing, shaping, and delays to assure comparator settling before a decision, and to avoid race problems.
- (3) Manual start or continuous conversion control (this would be supplied externally in an actual system application).

Complete Circuit

Figure 23 shows the complete SA A/D circuit, using a $\mu A741$ as the unity gain buffer amplifier. For higher speed inputs, a higher speed op amp should be used.

The total integrated circuits used are as follows:

PART NUMBER	QUANTITY
$\mu A722$	1
$\mu A741$	1
$\mu A710$	1
TT μ L9001	2
TT μ L9002	7
TT μ L9009	1
TT μ L9020	6
TT μ L9300	2
	21 for 10 bits

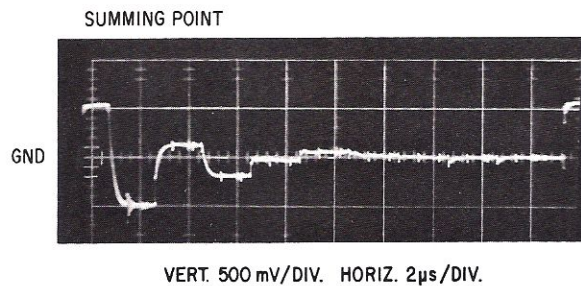


Fig. 24a. Comparator input.

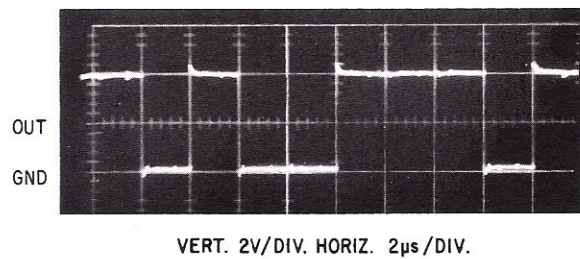


Fig. 24b. Digital output.

Fig. 24.

Performance

The system described is capable of conversion to 10-bit accuracy in 20 μ s, which is representative of the limitation imposed by the switching time of the least significant bits of the μ A722.

For 8-bit accuracy, the clock rate was increased such that the total conversion time was less than 10 μ s. Applying the recommended temperature coefficient considerations on the comparison amplifier, buffer amplifier, and μ A722 resistor array, 8-bit accuracy was readily held from 0 to +55°C.

Figures 24a and 24b show representative 2 μ s/bit waveforms for the ladder summation point and the digital output, respectively, for the 10-bit SA A/D converter using the μ A722.

OTHER SUBSYSTEM APPLICATIONS OF THE μ A722

A/D Converter: Extended Resolution and Accuracy

Resolution may be extended beyond 10 bits by cascading A/D converters. With reference to Figure 25, the operational amplifier multiplies the residual error voltage V_S to a level compatible with the second converter $I_S R_S$ full-scale. Tying the stabilization terminals in common will insure a nearly equal operating bias

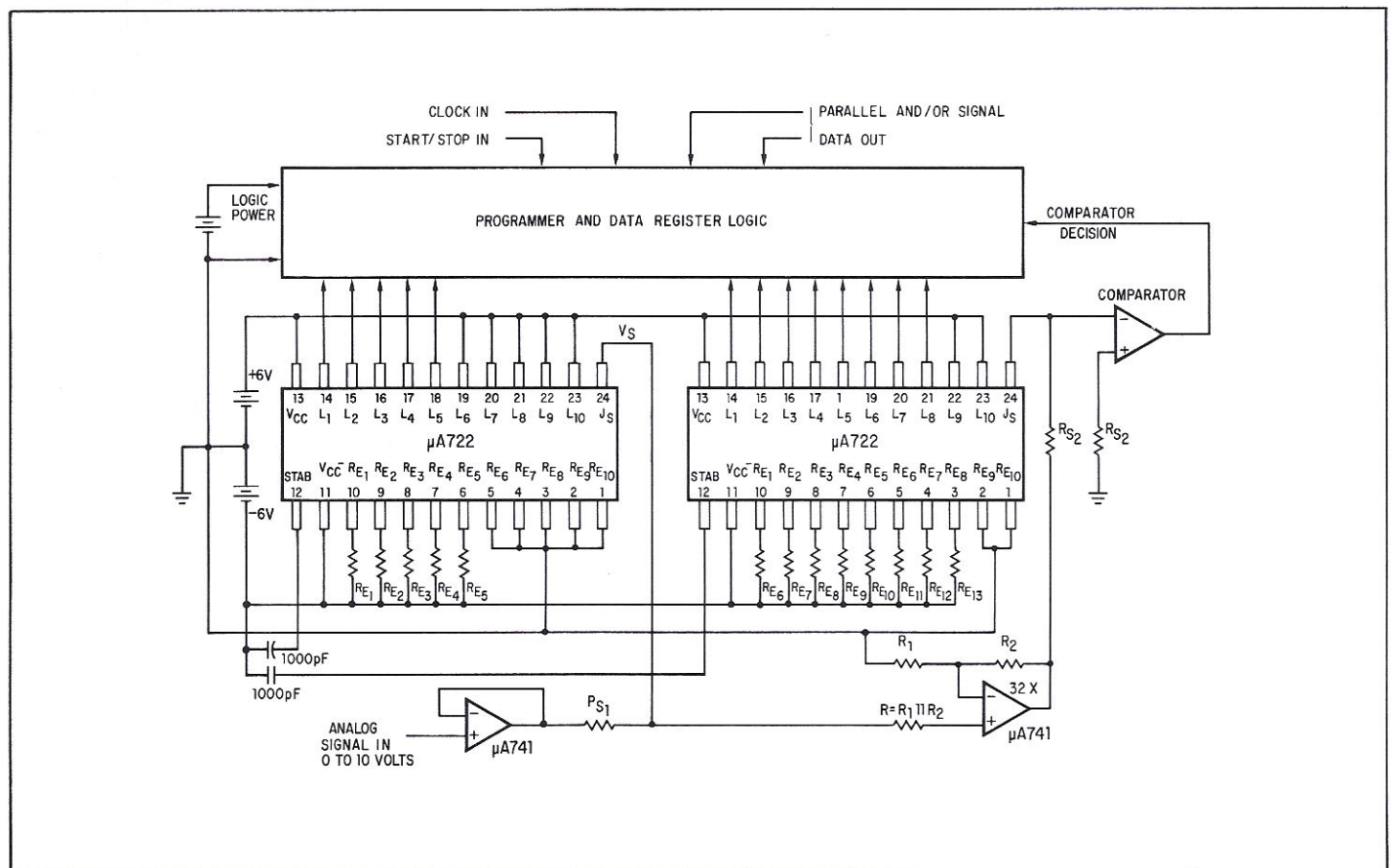


Fig. 25. High resolution analog-to-digital converter.

on each converter. The resolution of the system is limited by the system noise, with 13 to 15 bits being the maximum. This configuration is slower than a single - $\mu A722$ converter because of the slewing time required for the 32X amplifier.

A trade-off exists between the speed and accuracy achievable with the $\mu A722$ through the relation between current noise and sampling interval. The accuracy improvement is inversely proportional to the square root of the sampling interval, or bit time. An improvement of one bit is possible at 250 k bits, and 2 bits at 63 k bits. For this reason, the range of accuracy extends from 13 bits at one megabit to 15 bits at 63 k bits.

Accuracy equal to the resolution is attainable only by temperature control. Miniature ovens built by crystal oven manufacturers can hold temperature to $\pm 2^\circ\text{C}$ over the industrial range of 0°C to 70°C , and thus maintain fidelity to the original resistor settings within $\pm 0.01\%$. At temperatures in the upper military range, leakage current limits accuracy despite thermal control.

Higher Speed D/A

The $\mu A722$ can switch its 5th bit in 500 nsec to .05% accuracy. Therefore, two units driving separate operational amplifiers can be summed at 32:1 ratio by a third operational amplifier to provide reliable 10-bit operation at 500 nsec. This is shown schematically in Figure 26.

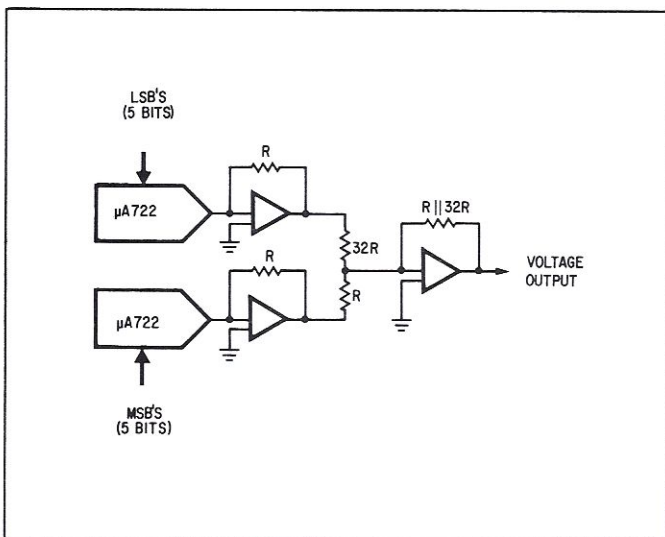


Fig. 26. High speed 10-bit D/A by 5-bit paralleling of $\mu A722$.

Function Generation

Numerous functions can easily be generated by setting the individual bit currents of the $\mu A722$ to match the desired function with the bits actuated sequentially. This simplifies the digital generator. Two or more converters operated in this manner may be paralleled for greater resolution. Of course, with the standard D/A configuration, any function can be generated digitally with high resolution. But the digital generator may be considerably more complex. In either case, the output is converted to a voltage by a feedback amplifier, and may be smoothed by use of a parallel feedback capacitor.

Logarithmic D/A Converter

The use of a transistor in the feedback loop in the standard DAC allows the formation of the natural logarithm of the digital input value (except 0 value). This is illustrated in Figure 27. * The $V_{BE} = \frac{kT}{q} \ln \frac{I_s}{I_O(T)}$ characteristic of the feedback transistor holds with excellent precision over the $\mu A722$ current range. The use of a $\mu A726$ temperature controlled pair minimizes temperature variation, balances out I_O , and permits setting the logarithmic base current with R_O . Nominally the base current would be $2.5 \mu\text{A}$, i.e., the least significant bit current. Amplification could be set so that the output voltage would increase 1 V for each doubling of the $\mu A722$ current. For example, the output voltage would then range from 0 V for $2.5 \mu\text{A}$ to 9 V for the full-scale current of 1.2775 mA.

$$[(2^9 - 1) \cdot 2.5 \mu\text{A} = 1.2775 \text{ mA}].$$

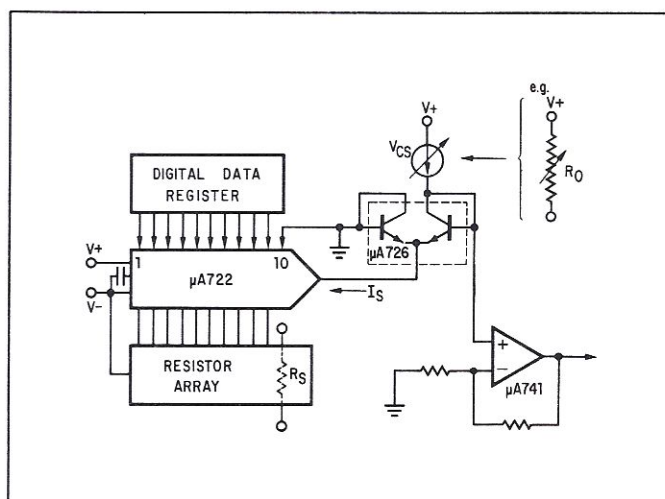


Fig. 27. 9-bit logarithmic D/A converter. Variable current source (VCS) should be adjusted for $E_O = 0$ with $I_S = 5 \mu\text{A}$. External resistor R_{10} should be equal to R_9 . For greatest thermal accuracy, R_S should be used to control the VCS.

D/A Multiplier

Hybrid multiplication or division can be accomplished at high speed with the $\mu A722$ in conjunction with a stable differential pair such as the $\mu A726$ (Fig. 28). It is easily shown for the pair that:

$$\Delta I_C = \frac{q}{2kT} I_S \Delta V_{BE} \quad (10)$$

$$\text{or} \quad \Delta E_{OUT} = K_1 I_S \Delta V_{BE} \quad (11)$$

$$\text{but} \quad I_S = E_{XD} \text{ and } \Delta V_{BE} = E_{XA} \quad (12)$$

$$E_{OUT} = K_2 E_{XD} E_{XA} \quad (13)$$

Thus the analog output is proportional to the product of the digital variable E_{XD} and the analog variable E_{XA} . Note that E_{XA} must be small to satisfy the differential equation above.

* For a more complete circuit, consult the Fairchild LIC Applications Handbook, pp. 150-152.

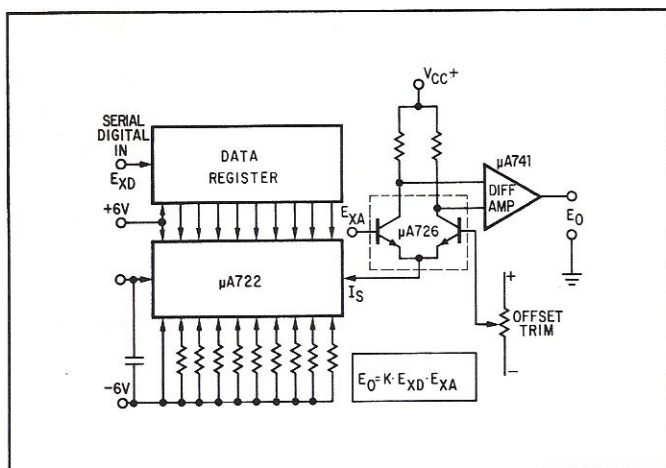


Fig. 28. Digital-to-analog multiplier.

Divider Circuit

The divider circuit, shown in Figure 29, makes use of the differential pair for multiplication. The output is fed back and multiplied with one of the data signals, E_X . This E_X is balanced with the second data signal, E_Y , by equating currents through operational amplifier action until

$$\frac{K_1 E_X E_O}{R_1} = \frac{E_Y}{R_2} \quad (14)$$

$$\text{or} \quad E_O = K_2 \frac{E_Y}{E_X} \quad (15)$$

E_Y may be a direct analog signal or one that is synthesized by D/A conversion.

III. SYSTEM APPLICATIONS OF μ A722 SUBSYSTEMS

Major areas of application for D/A and A/D converters and other subsystems described in the previous section occur in both digital and hybrid computer systems. This section briefly outlines the utility of the μ A722 in computer systems.

USES OF D/A AND A/D CONVERTERS FOR DIGITAL COMPUTER SYSTEMS

Introduction

A/D and D/A conversion requirements for analog equipment interfacing with digital computers vary greatly in speed and accuracy. Traditionally, higher word speed and accuracy are demanded of converters which measure analog signals (i.e., data acquisition ADCs) than are demanded of D/A converters for driving analog displays and controls. This is because:

- (1) High speed transient phenomena may have to be measured in real time (whereas they can be displayed in post time).
- (2) Multiple measurements are multiplexed for encoding by a single ADC, whereas DACs commonly are used singularly (for DC response, and because economics permit).
- (3) A/D measurement range is often intentionally employed wastefully for greater input flexibility, whereas analog output range tends to be standardized.
- (4) Analog displays are limited in accuracy by the resolving power of the analog display devices, and limited in speed by the writing response of the display device or by the flicker response of the eye.

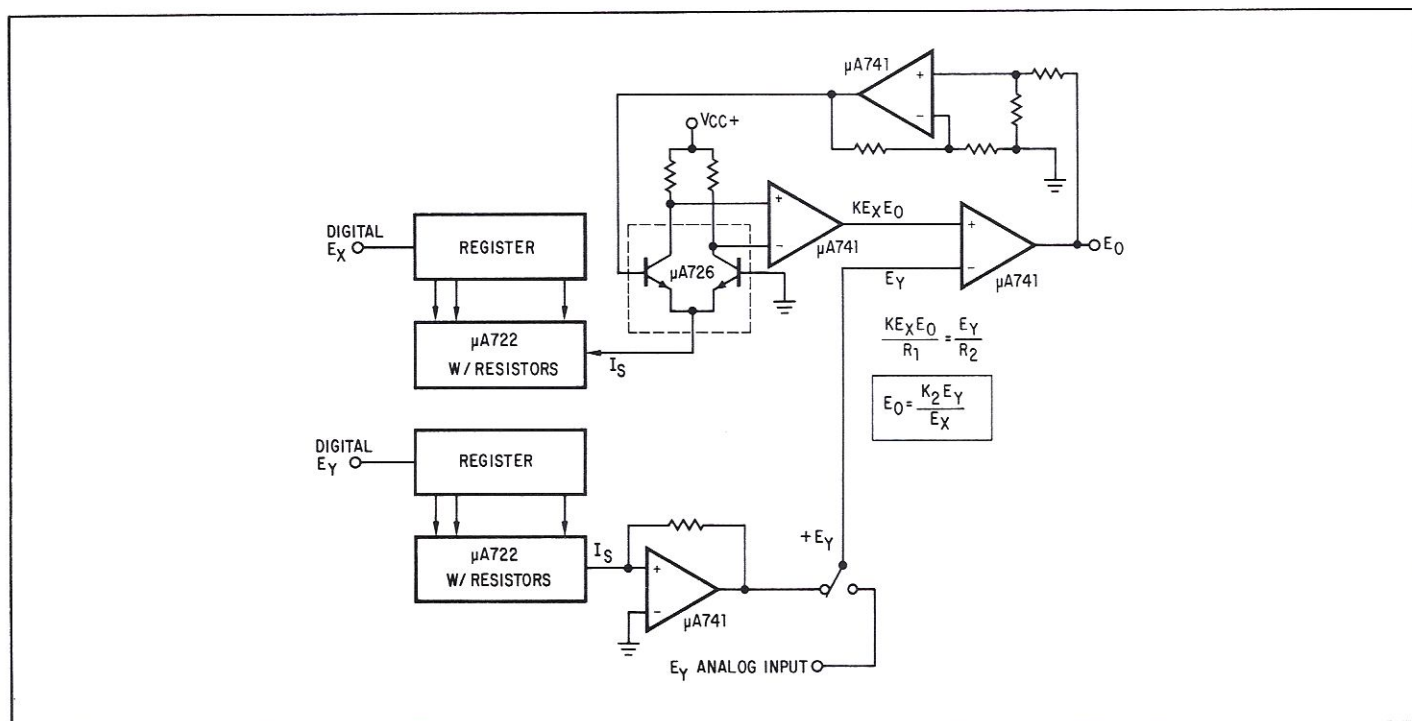


Fig. 29. Divider circuit.

Also, ADCs must operate at higher bit rates because they must operate bit-sequentially, whereas DACs can operate bit-parallel.

The purpose of this section is to relate the applicability of the $\mu A722$ on computer peripherals and computerized data acquisition systems.

Data Acquisition and I/O Requirements

The measurement and conversion of analog phenomena to digital quantities is often referred to as "data acquisition". For the purpose of entry into digital computers, a distinction must be made between real time and post time data acquisition. In real time acquisition, the speed of conversion must not be greater than the computer's input speed. In some cases, the instantaneous data rate may be faster than the computer I/O can accept, and the data must be buffered by a high-speed storage medium such as analog tape or peripheral core memory.

Storage and I/O Considerations

Typically, the data rate from high-accuracy ground data acquisition systems is less than 500 k bits/sec. If a buffer composes two words of data per computer word, this can be reduced to 50 k words/sec, which is within the capability of most computer multiplexers. Thus, the computer I/O can handle the data rates of acquisition systems, but storage capacity can be a problem. If greater than one second of data is to be stored at the above rate in core, the cost would be considered prohibitive---20,000 words of memory. Therefore, tape storage is commonly used.

The techniques which must be used for tape storage become more expensive and difficult as the data rate exceeds one megabit. At 1000 bits per inch and 150 inches per second, eight channels are necessary, including a clock, and a packing limitation begins to be reached because of the compromise which skew control demands between channel packing density and number of channels across a tape. Discs are faster than tape, but have less capacity.

For the above reasons, data acquisition rates above one megabit/sec are exceptional, and most requirements are within the nominal 1 megabit/sec capability of $\mu A722$ converters.

Data Scaling and Offset by Hybrid Techniques

Digital data measurement systems often require scaling and offset operations upon the samples. This can usually be performed in post time by the digital computer, but often taxes the operation rate of the computer for systems requiring real time usage of the data. In such cases, the D/A multiplying scheme described earlier can be used prior to A/D conversion to perform scaling, and a DAC - operational amplifier algebraic summer can be used to perform offset. This is shown in Figure 30, where the offset and the scaling numbers are derived from a digital table stored in the computer and brought out in blocks to a buffer. Scaling and offset can be performed in about two microseconds, one microsecond for DAC settling time and one microsecond for the arithmetic functions. Also, when necessary, high-speed division such as the ratio of two measurements can be performed by either of the two methods described earlier.

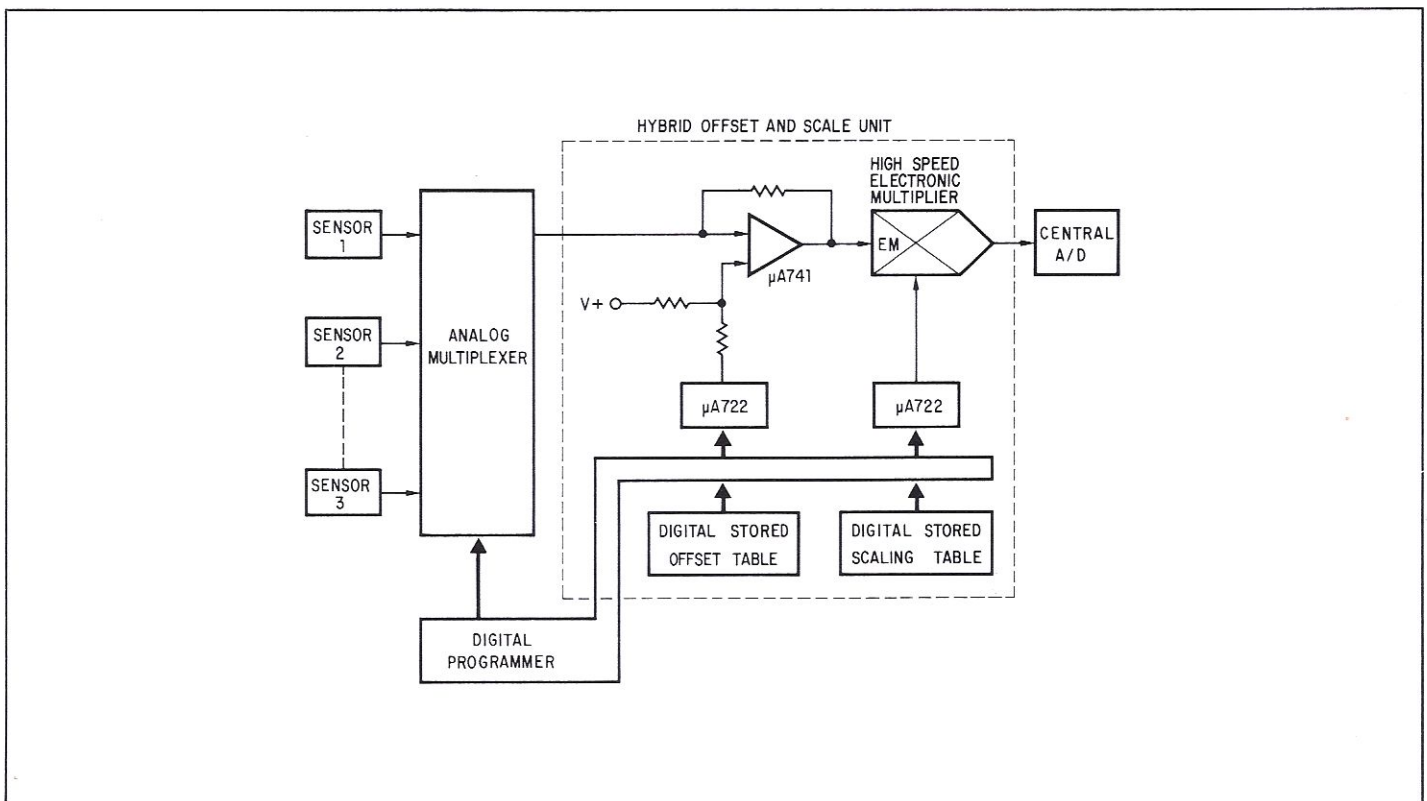


Fig. 30. Illustrative use of hybrid offset and scale computer (to reduce loading of the GP computer).

Local A/D Conversion

With the advent of miniature low-cost A/D conversion made possible by IC's, many systems designers are considering schemes involving local A/D conversion close to the signal generators and sensors. A major objective in such schemes is to reduce the staggering amount of cabling associated with high-accuracy measuring systems. Additional benefits are the increased reliability and simplified maintenance and check-out which result from avoiding dependence on a single A/D converter, as in conventional analog multiplexer approaches. Early applications of this technique are beginning to be seen in military aircraft data monitor systems. These systems detect incipient failure patterns by monitoring many data sources throughout the airplane and operating on the digitized readings with detection algorithms. Eventually, real time closure of the loop will provide protection against dangerous maneuvers with respect to the aircraft structure and stability, or dangerous conditions such as equipment burnout, overheating, over stressing, etc. As shown in Figure 31, a common set of output lines can be shared by all ADCs. Time multiplexing is accomplished by digital code selection as shown.

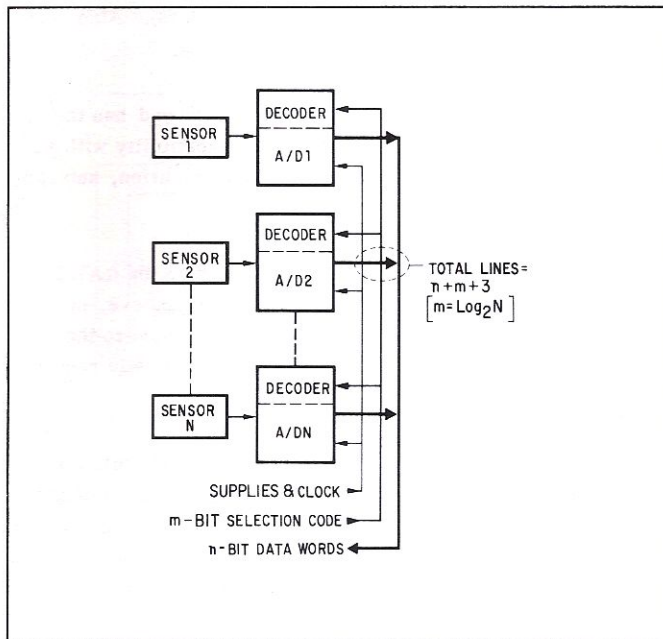


Fig. 31. Local ADC data acquisition system for cable reduction, reliability enhancement.

When cable reduction and economy are both paramount criteria, a compromise hybrid approach in which closely located sensor "clusters" are analog multiplexed into a local converter may be preferable. The speed of the $\mu A722$ readily permits handling clusters of 10 or more sensors.

Displays

The availability of low-cost integrated circuit D/A converters is expected to have important benefits in a number of areas in which analog displays are driven by digital computers. Although analog displays are less accurate than the digital type, they can be read and comprehended much faster in cases where

high accuracy is unnecessary. Even in cases where high accuracy is necessary, the deviation from the expected value can be displayed in an analog manner with superior human intelligibility. This is of particular importance to special-purpose operational systems employing digital computers, such as those used in aircraft and some ground control stations in which an operator must react quickly. Analog displays are also of great use to those data analysts editing digital data originally of an analog nature, such as in telemetry or picture transmission.

A major area of application is curve plotters such as strip-chart recorders and X-Y recorders or plotters. Here, an interesting competition exists between two techniques: (1) the stepping motor drive, and (2) the DAC-driven servo positioner. Lower cost DACs may have a major effect on the economic balance between these two techniques. The servo positioner is faster and is the sole method when higher speed plotting is required.

Low-cost DAC availability could trigger the abundant use of simple galvanometer needle meters. This is an application which, in the past, has been prohibitive in cost.

DACs are commonly used in the driving of cathode ray tube displays. Examples are light pen design consoles and computer-driven overlay displays for radar target tracking. These are driven by digitally generated sweeps for either X-Y positioning or symbol generation, or both. The speed requirement on the DACs for this type of application varies with the specific design and the time allocated for regeneration of the overlay display. Generally, one microsecond per sample is sufficient for a change in the X-Y coordinates as the speed limitation is primarily in the sweep circuits of the CRT. Other salient considerations in DAC-controlled CRT beam positioners are the high voltage and high current drive requirements. By the transimpedance op amp technique, the $\mu A722$ can readily drive special discrete component operational amplifiers intended for such service.

High Speed Analog Storage

The digital computer is capable of spewing out a sequential data list faster than high-speed mass storage media such as tape machines or discs can handle it. In such cases, high-speed D/A conversion can be performed and samples stored in analog fashion. (This obviously is applicable only to data which represents analog samples and whose accuracy is not critical, since good high-capacity analog storage media are limited to deposited magnetics, with attendant poor dynamic range and accuracy). For rates higher than 1 megabit, use of the first 5 bits can push the $\mu A722$ as high as 2 to 3 megawords/sec.

USES OF D/A AND A/D CONVERTERS FOR HYBRID COMPUTERS

Introduction

The new generation of A/D and D/A building blocks is expected to have a special impact on the economics of hybrid computers, especially with respect to the digital control of quasi-fixed or fixed analog parameters (viz., potentiometer settings and initial conditions). The three major areas of usage for analog-to-digital and digital-to-analog conversion in hybrid computers are: (1) D/A cross-conversion, (2) condition setting, and (3) high-speed arithmetic and function generation.

Cross Conversion

General purpose hybrid computers demand that errors from individual contributing sources be on the order of 0.01% so that overall error for a computation does not rise above 0.1%; therefore, conversion should be targeted for 13 or 14 bits. This is within the accuracy of the dual μ A722 converters. Normally, the DAC's speed will not be taxed, as all bits are converted in parallel. The speed requirement on A/D conversion can be difficult if multiplexers are used to sample many points in the analog portion of the system, or if the digital computer is especially fast in accepting data (e.g., through the use of multi-processors). A microsecond per bit is more than fast enough for A/D conversion if a single analog point is being converted in the analog portion of the hybrid system, because the analog portion will not accurately handle signals above 10 to 100 Hz.

Condition Setting

Whereas the use of A/D and D/A conversion is traditional in hybrid computers, separate digital storage of fixed analog parameters such as initial conditions and gain settings has not been common because of the expense. With the reduced costs made possible by ICs, each initial condition voltage can be injected by a separate DAC whose register digitally stores the setting. Similarly, amplifier gains can be adjusted and held by the DACs through the use of a circuit similar to that shown in Figure 28 for the analog multiplier. Even amplifier drift and offset can be removed by automated DAC zero-setting before each run.

Two interesting economic trade-offs will occur: (1) between (a) the use of higher priced, accurate DACs for initial condition setting as opposed to (b) the use of lower priced, inaccurate (but high resolution) DACs which are sequentially set by comparison against a high-accuracy reference; and (2) between (a) higher priced, low offset amplifiers, and (b) cruder, D/A-zeroed units.

High Speed Arithmetic and Mathematical Function Generation

The last advantageous application of the new low-cost, high-speed bipolar A/D and D/A integrated circuits is in the performance of high-speed hybrid arithmetic. Always available in a

hybrid computer is the capability of digitally performing mathematical functions of all kinds. However, some arithmetic functions such as division take considerable time in a digital computer, from 22 μ sec to perhaps as long as 100 μ sec. By the use of operational amplifiers and D/A current sources in conjunction with the multiplier circuit scheme described previously, it is possible to perform the functions of multiplication and division in from two to ten microseconds, and to accuracies in the range of 0.01% to 0.1%.

Typically, for multiplication, a microsecond is required for the D/A conversion and another microsecond for the analog signal multiplication. For division, if performed in the analog manner shown in Figure 29, a longer time is required because of the need for frequency compensation. If a digital successive approximation scheme is employed, the time is equivalent to A/D conversion, that is, about one microsecond per bit.

CONCLUSIONS

The μ A722 monolithic integrated circuit, in conjunction with other IC (or discrete) amplifiers, is capable of conversion at one microsecond per bit with accuracies approaching the best performing discrete component versions (13 to 15 bits). Also, very high speed conversion is possible by paralleling.

The D/A current source technique employed has the advantage not only of high speed, but also of compatibility with such operations as analog multiplication, division, addition, subtraction and function generation.

The speeds and accuracies achievable with the μ A722 are applicable to the I/O functions of GP digital computers, namely, data acquisition and displays, and are also applicable to the conversion, condition-setting, and high-speed arithmetic requirements of hybrid computers.

Finally, the low cost, simplicity, and reliability made possible by the existence of integrated circuit building blocks for A/D and D/A conversion will, with time, offer revolutionary system possibilities with respect to the economics of the above applications. This should have a special impact on the computing power versus cost of hybrid computing systems.

APPENDIX

Supply and Ground Lead Ringing Due to $\mu A722$ Current Switching

In discussing high speed applications of the $\mu A722$, two distinct cases arise:

- (1) The current summing bar is loaded by a low resistance ($\leq 200\Omega$) to ground.
- (2) The current summing bar potential is virtual ground; however, current does not come from ground but from the output stage of an operational amplifier.

The effect of switching on all the logic inputs is to steer the full-scale current (≈ 2.5 mA), which constantly flows in the current sources regardless of the logic state, from the V_{CC}^+ supply to the current summing bar. The net result is a 2.5 mA current step between the I_S and V_{CC}^+ terminals. (Actually there are several time-delayed steps, since the bits do not turn on simultaneously; however, bits 1 and 2, which account for 3/4 of the full-scale current, turn on in less than 10 nanoseconds). The equivalent circuit is shown in Figure 1 for case (1).

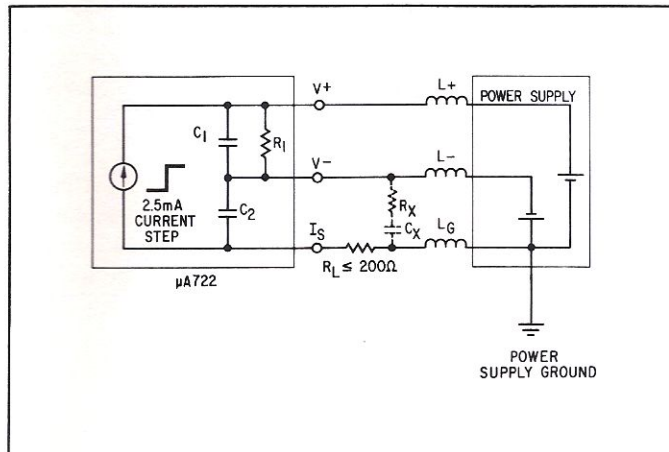


Fig. 1. Equivalent circuit with low resistance load on current summing bar.

$$R_1 = 1.8 \text{ k}\Omega; V_{CC}^- \text{ to } I_S \text{ resistance assumed infinite.}$$

$$C_1 \approx 125 \text{ pF} = \text{Collector substrate capacitance of } Q_{11} - Q_{30}, Q_{41} = Q_{45} \text{ and resistor boxes.}$$

$$C_2 \approx 70 \text{ pF} = \text{Collector substrate capacitance of } D_1 - D_{10} + \text{other capacitances, depending on whether the bit is on or off.}$$

L_+ , L_- , L_G are lead inductances from the power supplies to the $\mu A722$.

A Y- Δ transformation results in the circuit of Figure 2.

The effect of the current step will be to produce undesirable ringing currents through R_L . Both loop (1) and (2) will ring.

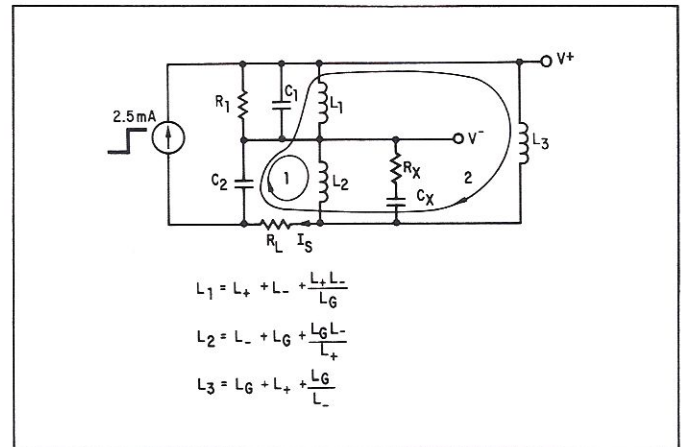


Fig. 2.

A small resistor R_X ($\approx 50\Omega$) in series with a capacitor C_X (≥ 1000 pF) for DC isolation will damp both loop currents sufficiently. The damping time constant for loop (1) will be approximately $R_X C_2$ or 3.5 nsec. For loop (2), the impedance of the $R_X C_X$ series combination will be considerably less than that of L_L, C_2 ; hence, a large percentage of the loop current has been diverted from R_L .

For case (2), R_L is replaced by an operational amplifier as shown in Figure 3.

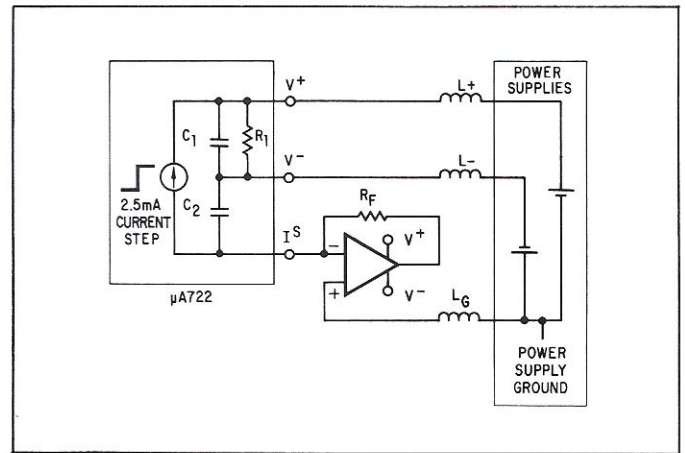


Fig. 3. Equivalent circuit with operational amplifier load on current summing bar.

The basic difference between the two cases is that there is no appreciable current flow into the non-inverting terminal of the op amp and therefore L_G is negligible.

Since the response of the operational amplifier is limited by its slewing rate, it will not be able to supply the current required by the $\mu A722$ instantaneously; i.e., the equivalent circuit will be as shown in Figure 4.

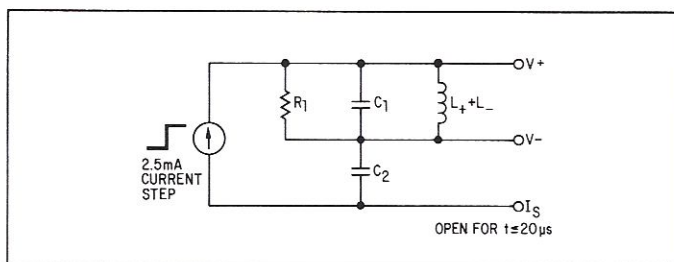


Fig. 4.

The $V^+ - V^-$ waveform will be

$$V^+(t) - V^-(t) \approx 2.5 \text{ mA} \sqrt{\frac{L_+ + L_-}{C_1}} e^{-\frac{t}{2R_1 C_1}} \sin \frac{t}{\sqrt{(L_+ + L_-) C_1}}$$

The time constant ($2R_1 C_1 \approx .45 \mu\text{sec}$) does not provide sufficient damping if the lead inductances are too high, notwithstanding the fact that the power supply rejection of the μA722 improves at high frequencies compared to the DC value.

A similar effect occurs with the operational amplifier. A current ramp, the slope of which is determined by the slew rate, can cause ringing as it flows into the V^+ supply. Since op amp power supply rejection falls off at high frequencies, this ringing will show up at the output.

Both of these effects can be damped sufficiently by a small resistor, R_s , in series with the supply leads. The damping time constant is $2L/R_s$, which will be small enough for reasonable lead inductances.

Since the μA722 and the op amp are in close physical proximity, the same supply can be used for both. This will result in only one ringing circuit. Furthermore, switching all logics on effectively steers 25 mA from the μA722 V^+ supply to the operational amplifier V^+ supply, which are tied together; therefore, there is no net change in V^+ supply DC current.

Both the μA722 and op amp can be operated off ± 9 V supplies, or zener diodes can be used to drop from ± 12 V or ± 15 V for the op amp, or to ± 6 V for the μA722 .

